Top assembly

Component placement, fitted-side orientation and 3D reference

ASSEMBLY NOTES

01 View from outside the top of the board. Use the PCB outline and connector edges to orient the board.

02 Reference plan is 1:1.36 at A3 / 100% print (170 mm board shown 125 mm wide). 3D illustration is not a dimensional drawing.

03 Teal outlines identify pad 1 / A1. Verify device polarity and pin numbering against the footprint and datasheet.

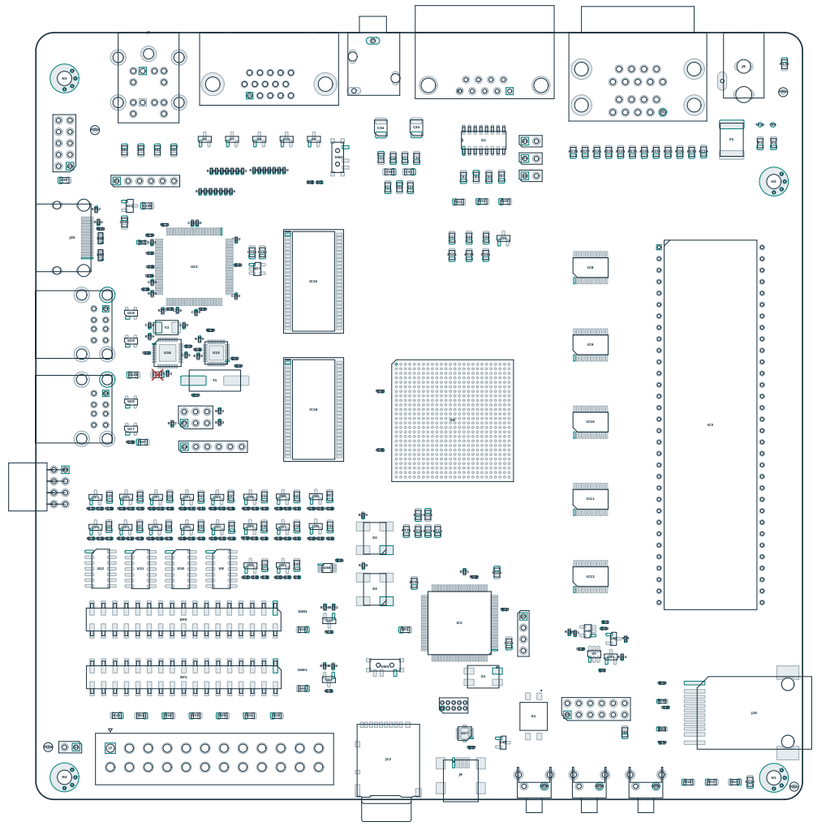
04 Red crosses mark DNP footprints. The BOM controls population and component values.

05 SAMV71 recovery provides SWD, NRST and ERASE access. New ARM firmware and Spartan-7 FPGA ports are required for this revision.

06 IC15 and IC16 are 64 MiB each, on independent 16-bit SDRAM buses. IC17 and IC18 complete the bottom-side 68000 translators.

07 FID1-4 are on top; FID5-8 are on the bottom. Native footprints control fiducial geometry. Markers are excluded from the purchasing BOM.

REFERENCE PLAN / 1:1.36

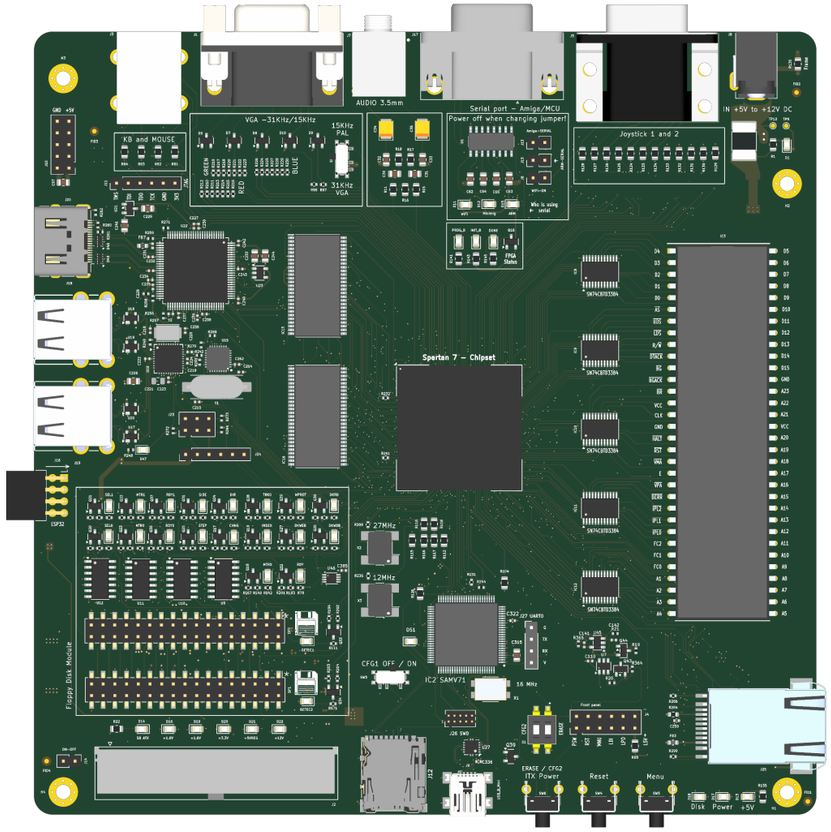


25 mm print scale check

FID1: X 298.050, Y 219.760 mm (native top view)

FID2: X 295.600, Y 65.800 mm (native top view)

3D ASSEMBLY VIEW



ASSEMBLY INVENTORY

Placement	Footprints	SMD attr.	DNP
Top side	349	315	1
Bottom side	492	480	14

KEY DEVICES

Reference	Role	Device
U8	FPGA / BGA676	XC7S100-FGGA676
IC2	Control MCU	ATSAMV71N20B-AAB
U26	Ethernet controller	ENC624J600-I/PT
U22	HDMI transmitter	IT6613E

Bottom assembly

Component placement, fitted-side orientation and 3D reference

ASSEMBLY NOTES

01 View from outside the bottom of the board. Bottom drawing is mirrored left to right.

02 Reference plan is 1:1.36 at A3 / 100% print (170 mm board shown 125 mm wide). 3D illustration is not a dimensional drawing.

03 Teal outlines identify pad 1 / A1. Verify device polarity and pin numbering against the footprint and datasheet.

04 Red crosses mark DNP footprints. The BOM controls population and component values.

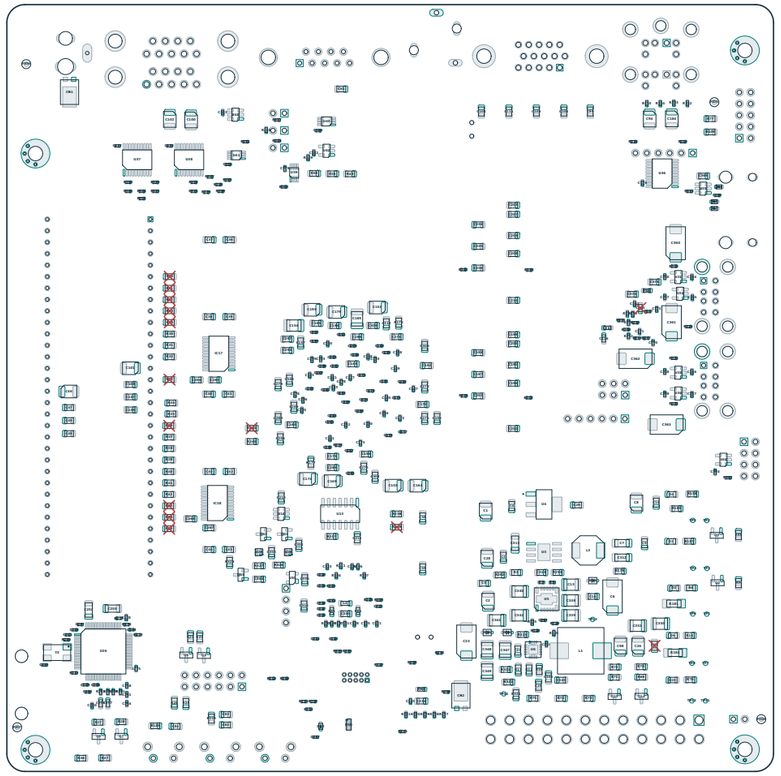
05 SAMV71 recovery provides SWD, NRST and ERASE access. New ARM firmware and Spartan-7 FPGA ports are required for this revision.

06 IC15 and IC16 are 64 MiB each, on independent 16-bit SDRAM buses. IC17 and IC18 complete the bottom-side 68000 translators.

07 FID1-4 are on top; FID5-8 are on the bottom. Native footprints control fiducial geometry. Markers are excluded from the purchasing BOM.

08 D58, C368 and U36 have been repositioned to increase clearance from through-hole copper. The reference plan and 3D view show the updated placement.

REFERENCE PLAN / 1:1.36

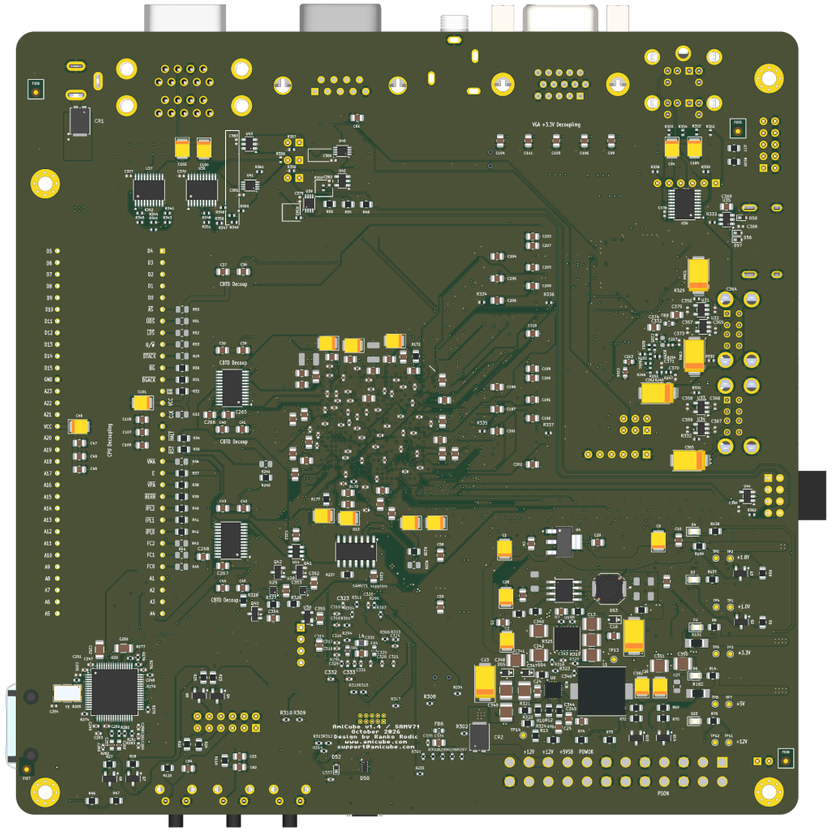


25 mm print scale check

FID5: X 143.020, Y 74.230 mm (native top view)

FID6: X 295.600, Y 65.800 mm (native top view)

3D ASSEMBLY VIEW



Frame0-CONNECTED MOUNTING HOLES

Ref	Hole	X	Y
H1	3.2	163.65	165.20
H2	3.2	163.65	33.02
H3	3.2	6.35	10.16
H4	3.2	6.35	165.10

Four 3.2 mm clearance holes. 170 × 170 mm outline with R4 corners; saved thickness 1.656 mm.

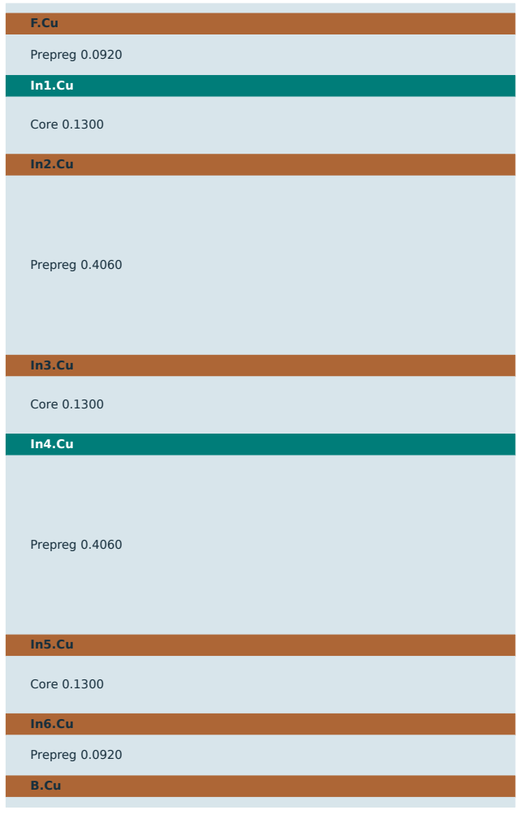
Coordinates are measured from the top-view upper-left outline tangent, +X right and +Y down. Bottom illustration is mirrored; this coordinate table remains in top-view coordinates.

Stackup & fabrication

Saved laminate definition, layer allocation and actual through-via inventory

8 LAYERS / SAVED 1.656 mm

Cross-section: thickness exaggerated



Layer	Material / construction	t (mm)	Er	Df	Function
F.Mask	Solder mask	0.01	—	—	Coating
F.Cu	Copper	0.035	—	—	Signals / components
dielectric 1	3313 RC57%	0.092	4.1	0.02	Insulation
In1.Cu	Copper	0.03	—	—	GND reference
dielectric 2	NP-155F core	0.13	4.17	0.02	Insulation
In2.Cu	Copper	0.03	—	—	Signals / power
dielectric 3	2 x 7628 RC49%	0.406	4.4	0.02	Insulation
In3.Cu	Copper	0.03	—	—	Signals / power
dielectric 4	NP-155F core	0.13	4.17	0.02	Insulation
In4.Cu	Copper	0.03	—	—	GND reference
dielectric 5	2 x 7628 RC49%	0.406	4.4	0.02	Insulation
In5.Cu	Copper	0.03	—	—	Signals / 3.3 V
dielectric 6	NP-155F core	0.13	4.17	0.02	Insulation
In6.Cu	Copper	0.03	—	—	Power / local GND
dielectric 7	3313 RC57%	0.092	4.1	0.02	Insulation
B.Cu	Copper	0.035	—	—	Signals / components / GND
B.Mask	Solder mask	0.01	—	—	Coating

Sum of saved thickness entries: 1.656 mm including masks; 1.636 mm without masks.

Laminate: NP-155F / JLC081611-3313. Saved copper: 0.035 mm outer / 0.030 mm inner.

Native copper-finish field: ENIG. Manufacturing release remains pending.

THROUGH-VIA INVENTORY

Land Ø	Drill Ø	Annulus	Count
0.3	0.15	0.075	1962
0.4	0.2	0.100	273
0.45	0.2	0.125	10
0.45	0.25	0.100	8
0.5	0.2	0.150	30
0.5	0.25	0.125	3
0.6	0.3	0.150	113
1	0.5	0.250	2

FABRICATION REVIEW NOTES

Outline: 170 × 170 mm, R4 corners. Four 3.2 mm mounting holes. 2,401 routing vias; minimum recorded drill 0.15 mm. Mounting-ring drills are counted separately.

In1 and In4 carry the ground-reference pours. In6 includes split supply copper and local ground; do not assume an unbroken ground plane.

U6: four 0.45 / 0.25 mm thermal vias require resin fill and copper caps (IPC-4761 Type VII). Confirm with the fabricator; archived production files predate this circuit.

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Design documentation • 1.4-routed • 2026-10-21 • source d33b543be0ea

Units: mm. Saved CAD and BOM govern. Renders are illustrative; no bench qualification implied.

Routing & impedance

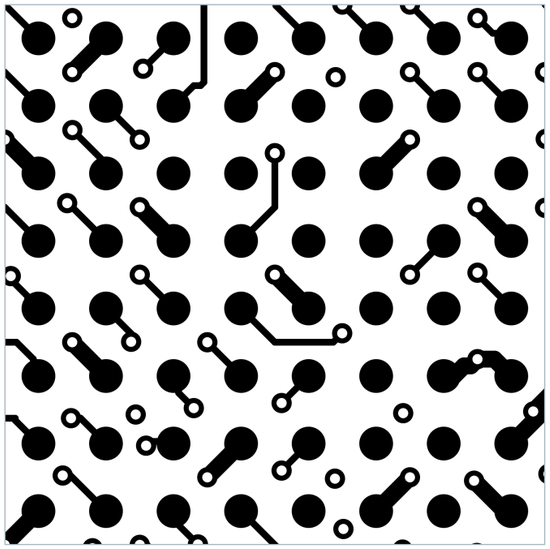
Current differential-pair targets and local BGA rules — main project

Circuit / class	Scope	Width	Gap	Target Zdiff	Notes
Digital data / control	All routing layers	0.100	—	Uncontrolled	Includes both SDRAM channels and clocks
BGA fanout / data	Under U8 / all Cu	0.100	—	Uncontrolled	Same signal width inside and outside FPGA fanout
U8 supply escape	U8 courtyard / all Cu	0.250	—	—	Local 1.0 V / 1.8 V / 3.3 V; wider feeders allowed
USB differential	Outer layers	0.130	0.160	90 ohm	U15 MAX3421E host / U16 USB2514B hub; service USB
USB hub pair	In2.Cu	0.130	0.170	90 ohm	In1 reference / In4 distant reference
HDMI TMDS	Outer layers	0.100	0.160	100 ohm	IT6613E; R260/261 = 1.8k DDC, R262 = 10k HPD
Ethernet RX / TX	Outer layers	0.100	0.160	100 ohm	ENC624J600 to the current J25 location

Impedance values are nominal design targets; no new field-solver, TDR or timing qualification is implied.

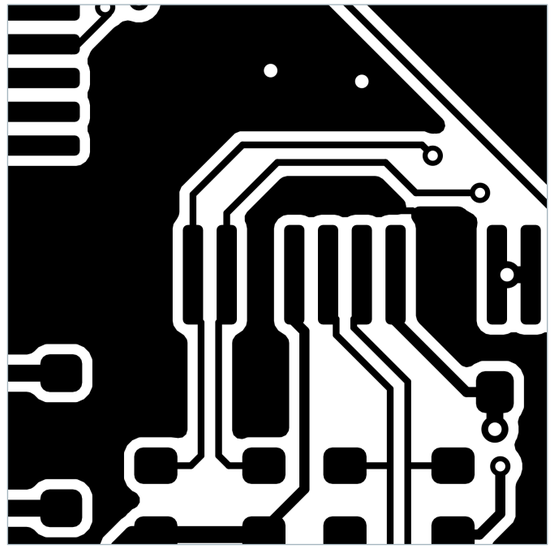
Pair-gap minimum: 0.15 mm. Optimum: 0.16 mm outer / 0.17 mm inner USB. Native custom rules govern.

A / BGA ESCAPE DETAIL



F.Cu / 11:1 — native filled copper

B / ETHERNET CONTROLLER DETAIL



B.Cu / 11:1 — top-view coordinates

Native copper detail, including adjacent nets

REFERENCE PLANES & PAIR GEOMETRY



Illustration only — not to scale

F.Cu references In1 ground. Bottom differential routes rely on local In6 ground. In2 USB uses In1 with In4 as the distant second reference.

HDMI has TMDS protection and D56–D58 clamps on DDC / HPD. Connector transient and system ESD testing remain pending; see the 21 October corrections.

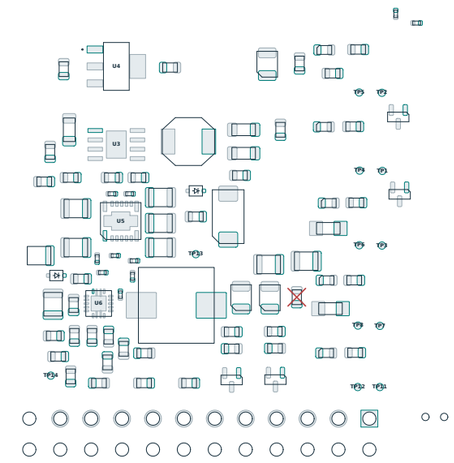
IC15 and IC16 have independent 16-bit buses. Their shared supplies do not make their clocks, address or command nets common.

Keep return paths continuous when editing. Width / gap rules are in AmiCube-v1.kicad_dru; FPGA timing and hardware tests remain pending.

Power & signal identification

Supply probes, CPU rail interlock and saved bus colours

REGULATOR / TEST-POINT LOCATOR



Bottom view / 1.2:1 / mirrored

D16 / D19 / D20 / D21 indicate the nominal rails. D44 / D45 / D46 show FPGA PROG_B / INIT_B / DONE circuit states.

LEDs do not qualify ripple, voltage accuracy or firmware operation.

REGULATED RAILS & INPUT

Nominal rail	Regulator / input	Indicator	Probe + / GND
+1.0V	U3 / BD9C401EFJ-E2	D16	TP1 / TP4
+1.8V	U4 / TLV76118DCYR	D19	TP2 / TP5
+3.3V	U5 / TPSM53604RDAR	D20	TP3 / TP6
+5VREG	U6 / TPS54622RHLR	D21	TP7 / TP8
12V-Supply	Rectified input / before F1	D22 / D23	TP11 / TP12

Listed probe pairs are on the bottom. Top-side input: TP10 (+12 V) / TP9 (GND). U5 is a 4 A-rated module; U6 is a 6 A IC with a 4 A board target. Board loads need bench qualification.

PGOOD probes (bottom): TP13 = SUPPLY3V3_PGOOD; TP14 = SUPPLY5V_PGOOD.

CPU POWER GUARD & RESET RELEASE

U28 / U29 qualify 5 V and 3.3 V; R328 defaults CPU translators and peripheral buffers OFF. U30 with Q41 / Q42 holds RESET and HALT separately for 140–280 ms after bus connection. Release also requires MCLR, PROG_B_UP, DONE and FPGA_CPU-RST.

The FPGA port must hold CPU reset until its clock, SDRAM and boot image are ready. The hardware guard qualifies rails; it does not detect a running CPU clock.

USB & HDMI POWER PROTECTION

U31–U34 TPS2051C switches protect the four USB ports. U35 TPS2553 limits HDMI 5 V and is enabled by CPU_RAILS_READY.

Clocks are yellow; SDRAM channels use separate palettes. Overview buses group signals visually; individual global labels carry cross-sheet connections.

BUS COLOUR KEY

- 68000 address
- 68000 control
- 68000 data
- Analogue audio
- Analogue video
- Clocks
- Digital single signals
- Ethernet RX pair
- Ethernet TX pair
- Ethernet address
- Ethernet control
- Ethernet data
- FPGA SPI
- FPGA configuration
- Floppy
- HDMI TMDS clock
- HDMI TMDS data 0
- HDMI TMDS data 1
- HDMI TMDS data 2
- HDMI blue data
- HDMI green data
- HDMI red data
- JTAG
- Joystick A
- Joystick B
- SD card
- SDRAM1 address
- SDRAM1 control
- SDRAM1 data
- SDRAM2 address
- SDRAM2 control
- SDRAM2 data
- System reset
- USB host SPI
- USB host pair
- USB hub pair
- USB port 1 pair
- USB port 2 pair
- USB port 3 pair
- USB port 4 pair
- USB service pair
- VGA blue data
- VGA green data
- VGA red data
- Video control

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Units: mm. Saved CAD and BOM govern. Renders are illustrative; no bench qualification implied.

AmiCube 1.4-routed / Power & signal identification

A3 · 2026-10-21 · Drawing 5/5