# Top assembly

Placement plan, fitted-side orientation and native 3D reference

## ASSEMBLY NOTES

01 View from outside the top. Orient using the board outline and connector edges.

02 Reference plan: 1:2 at A4 / 100%. The 170 mm board is drawn 85 mm wide.

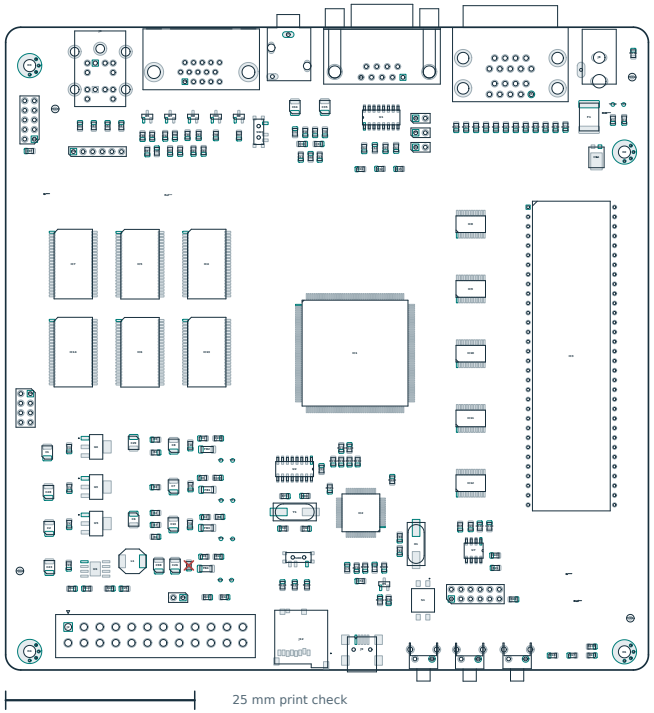
03 Teal marks pad 1 / A1. Check polarity and pin numbering against the footprint.

04 Red crosses mark saved DNP values. There are 18 options; native DNP flags are unset.

05 IC1: Spartan-3. IC2: ARM controller. IC3: MC68000. IC8-12: bus translation.

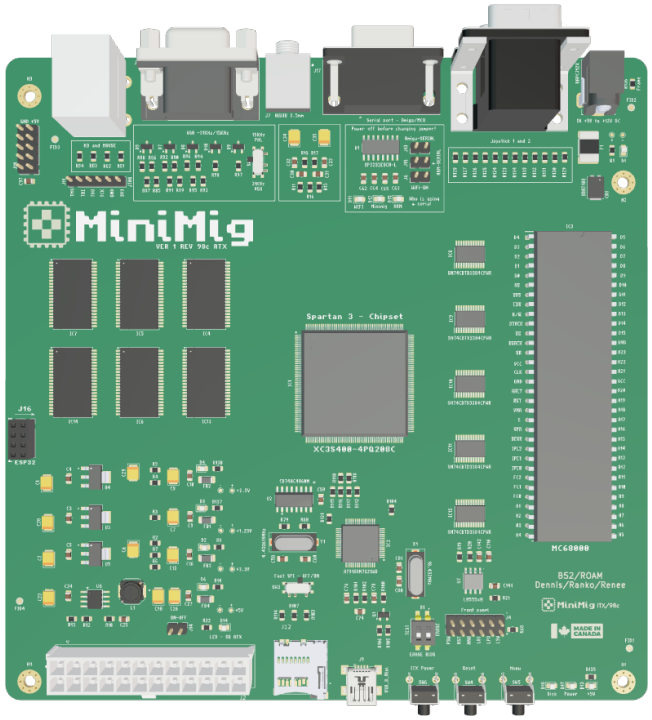
06 IC4-7 / IC13-14: six SRAMs, 6 MiB total. Shared 16-bit data and 19 address signals.

## REFERENCE PLAN / 1:2



25 mm print check

## 3D ASSEMBLY VIEW




| Side | Qty | SMD | DNP |
|---|---|---|---|
| Top | 217 | 172 | 1 |
| Bottom | 175 | 175 | 17 |

| Ref | Role | Device |
|---|---|---|
| IC1 | FPGA / PQ208 | XC3S400-4PQ208C |
| IC2 | Controller | AT91SAM7S256D |
| IC3 | CPU / DIP64 | MC68000 |

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Revision 1.98itx | 2026-10-17 | PCB 2d3f20eb0dd8

Units: mm. Saved CAD governs. 3D views are illustrative.

A4 landscape. Print at 100% for the stated drawing scales.

Minimig 1.98itx / Top assembly

A4 · 2026-10-17 · Drawing 1/5

# Bottom assembly

Placement plan, fitted-side orientation and native 3D reference

## ASSEMBLY NOTES

01 View from outside the bottom. Bottom view is mirrored left to right.

02 Reference plan: 1:2 at A4 / 100%. The 170 mm board is drawn 85 mm wide.

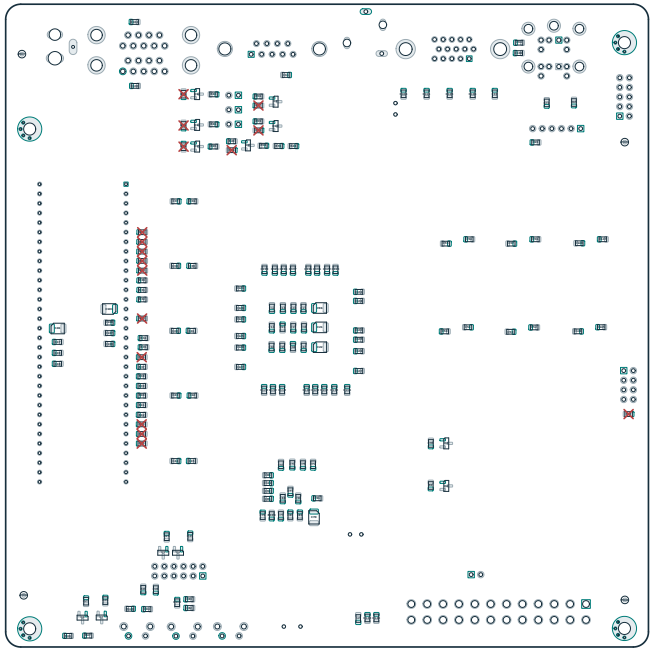
03 Teal marks pad 1 / A1. Check polarity and pin numbering against the footprint.

04 Red crosses mark saved DNP values. There are 18 options; native DNP flags are unset.

05 IC1: Spartan-3. IC2: ARM controller. IC3: MC68000. IC8-12: bus translation.

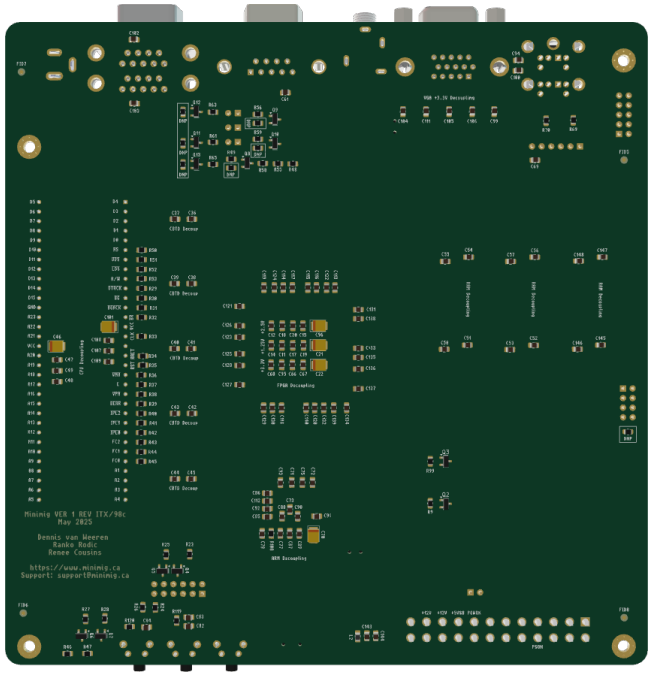
06 IC4-7 / IC13-14: six SRAMs, 6 MiB total. Shared 16-bit data and 19 address signals.

## REFERENCE PLAN / 1:2



25 mm print check

## 3D ASSEMBLY VIEW



| Ref | Drill | X | Y |
|---|---|---|---|
| H1 | 3.2 | 163.65 | 165.20 |
| H2 | 3.2 | 163.65 | 33.02 |
| H3 | 3.2 | 6.35 | 10.16 |
| H4 | 3.2 | 6.35 | 165.10 |

Mounting holes H1-4 connect to Frame0. Outline: 170 × 170 mm, R4 corners; nominal thickness 1.6 mm. FID1-4 are on top; FID5-8 are on the bottom.

Hole coordinates use the top-view upper-left outline tangent: +X right, +Y down. This table is not mirrored.

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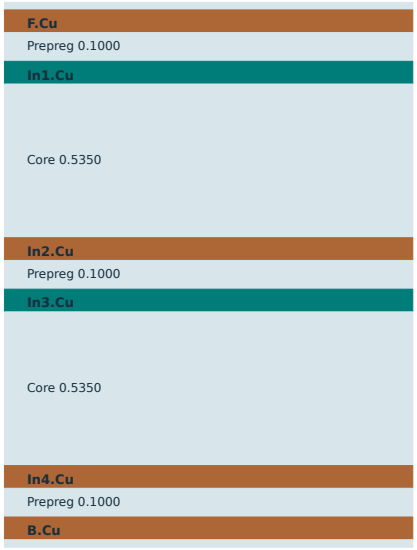
A4 landscape. Print at 100% for the stated drawing scales.

# Stackup & fabrication

Saved laminate definition, copper allocation and through-via inventory

## 6 COPPER LAYERS

Thickness exaggerated




| Layer | Material | t (mm) | Er | Df | Saved role |
|---|---|---|---|---|---|
| F.Mask | Mask | 0.01 | — | — | Coating |
| F.Cu | Copper | 0.035 | — | — | Signals / power |
| dielectric 1 | FR4 | 0.1 | 4.5 | 0.02 | Insulation |
| In1.Cu | Copper | 0.035 | — | — | GND reference |
| dielectric 2 | FR4 | 0.535 | 4.5 | 0.02 | Insulation |
| In2.Cu | Copper | 0.035 | — | — | Signals / power |
| dielectric 3 | FR4 | 0.1 | 4.5 | 0.02 | Insulation |
| In3.Cu | Copper | 0.035 | — | — | GND reference |
| dielectric 4 | FR4 | 0.535 | 4.5 | 0.02 | Insulation |
| In4.Cu | Copper | 0.035 | — | — | Signals / power |
| dielectric 5 | FR4 | 0.1 | 4.5 | 0.02 | Insulation |
| B.Cu | Copper | 0.035 | — | — | GND label; signal routing |
| B.Mask | Mask | 0.01 | — | — | Coating |

Thickness sum: 1.600 mm with masks; 1.580 mm without masks.

FR4: Er 4.5 / Df 0.02. All copper layers: 0.035 mm.

Saved finish: None. No specific laminate or impedance target.

## THROUGH VIAS

| Land Ø | Drill Ø | Annulus | Count |
|---|---|---|---|
| 0.45 | 0.2 | 0.125 | 767 |

In1 and In3 are ground references. B.Cu is named GND but also carries signals; inspect copper and return paths. Confirm stack, finish and drill capability before fabrication.

767 routing vias. Component and mounting drills are separate.

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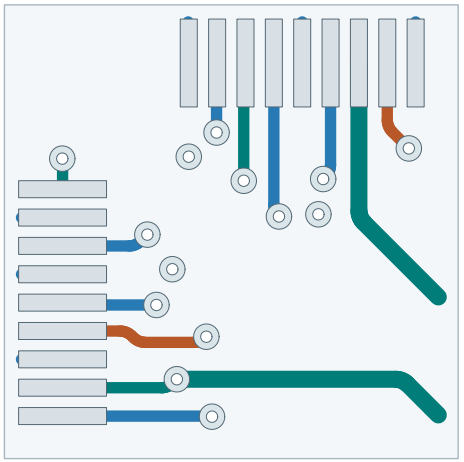
# Routing & impedance

Saved widths and native copper details; dimensions in millimetres

| Circuit / rule | Width | Gap | Saved evidence |
|---|---|---|---|
| MC68000 bus | 0.200 | — | 49 used channels through IC8-12 |
| Asynchronous SRAM | 0.200 | — | Six devices; shared address and 16-bit data bus |
| VGA RGB / sync | 0.200 | — | Four resistor-DAC bits per colour |
| USB service D+ / D− | 0.200 | — | Mini-B J9 to ARM IC2; VBUS unconnected |
| Default netclass | 0.250 | 0.250 | Clearance 0.150; diff-pair width 0.200 |
| Power / minimum | 0.200–3.000 | — | Power widths vary; minimum rule 0.200 |

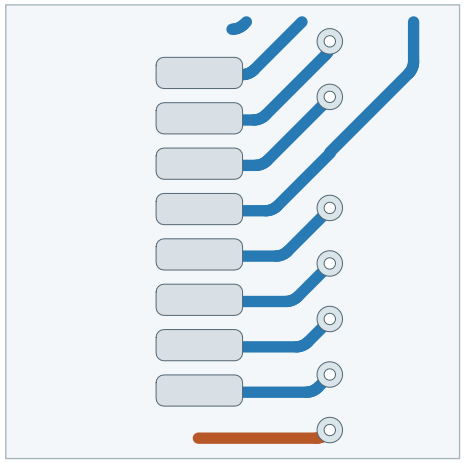
No per-interface impedance target is saved. Colours identify nets; they do not impose routing constraints.

## A / FPGA LEAD ESCAPE



F.Cu / 7.5:1

## B / SRAM BUS DETAIL



F.Cu / 7.5:1; native curves

## REFERENCE PLANES

In1 and In3: ground reference. F.Cu, In2 and In4: signals and power. B.Cu also has signal routing.

SRAM: RAM_D0–15, RAM_A1–19 and separate RAM_SEL0–5 selects. There is no SDRAM clock interface.

Preserve return paths and decoupling. These details record geometry; they do not establish skew, matched lengths or impedance.

Blue: signals

Orange: power; teal: ground

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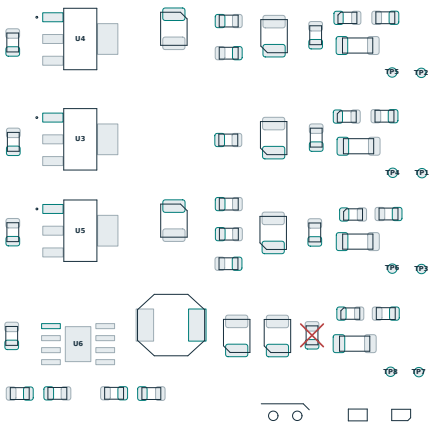
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A4 landscape. Print at 100% for the stated drawing scales.

# Power & signal identification

Regulated-rail probe points, indicators and drawing colours

## REGULATOR / PROBE LOCATOR




Top view / 1.25:1

## RAILS & INPUT

| Nominal rail | Regulator | LED | Probe + / GND |
|---|---|---|---|
| +1.25V | U3 | D3 | TP1 / TP4 |
| +2.5V | U4 | D4 | TP2 / TP5 |
| +3.3V | U5 | D2 | TP3 / TP6 |
| +5VREG | U6 | D6 | TP7 / TP8 |
| 12V-Supply | Input | D1 | TP10 / TP9 |

All probe pairs are on top. TP10 (+12 V) / TP9 (GND) are beside the barrel input. Rail names are nominal values, not acceptance tolerances.

D14: ATX standby. U7 / 5VSB: ATX control. Mini-USB VBUS is unconnected. J10 supplies +5VREG / GND despite its saved Spare I/O value.

## BUS COLOUR KEY

- Power rails
- Ground / return
- MC68000 interface
- Shared SRAM bus
- FPGA / ARM control
- Video / sync
- Stereo audio
- Joystick / PS/2 / serial

Drawing colours are reading aids. The saved project has one Default netclass with transparent colour fields. Named nets and pin connectivity govern.

Input: 12 V via J2 ATX or J8 barrel. Simultaneous-source operation is not specified.

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