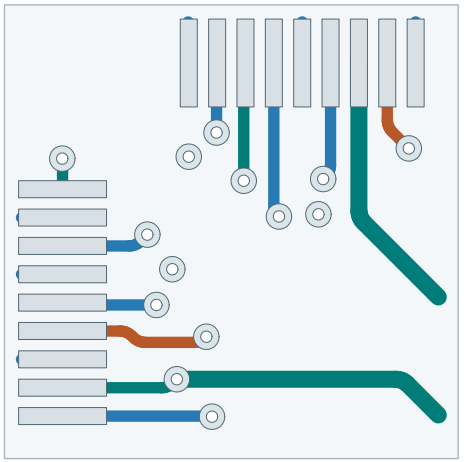
Routing & impedance

Saved widths and native copper details; dimensions in millimetres

Circuit / rule	Width	Gap	Saved evidence
MC68000 bus	0.200	—	49 used channels through IC8-12
Asynchronous SRAM	0.200	—	Six devices; shared address and 16-bit data bus
VGA RGB / sync	0.200	—	Four resistor-DAC bits per colour
USB service D+ / D−	0.200	—	Mini-B J9 to ARM IC2; VBUS unconnected
Default netclass	0.250	0.250	Clearance 0.150; diff-pair width 0.200
Power / minimum	0.200–3.000	—	Power widths vary; minimum rule 0.200

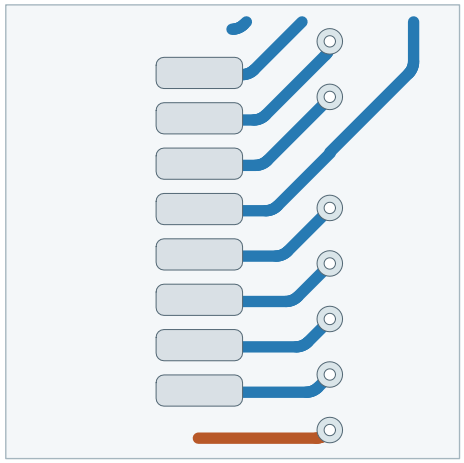
No per-interface impedance target is saved. Colours identify nets; they do not impose routing constraints.

A / FPGA LEAD ESCAPE



F.Cu / 7.5:1

B / SRAM BUS DETAIL



F.Cu / 7.5:1; native curves

REFERENCE PLANES

In1 and In3: ground reference. F.Cu, In2 and In4: signals and power. B.Cu also has signal routing.

SRAM: RAM_D0–15, RAM_A1–19 and separate RAM_SEL0–5 selects. There is no SDRAM clock interface.

Preserve return paths and decoupling. These details record geometry; they do not establish skew, matched lengths or impedance.

Blue: signals

Orange: power; teal: ground

Dennis, Ranko, Renee / Minimig.ca / Precision-Arrays

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Units: mm. Saved CAD governs. 3D views are illustrative.

A4 landscape. Print at 100% for the stated drawing scales.