System overview

Power

Sheet 2

Power input, protection and rails

{B_POWER} {B_POWER}

FPGA

Sheet 6

Spartan-3, clocks and memory

{B_FPGA} {B_FPGA}

Control

Sheet 15

MC68000, ARM and storage

{B_CONTROL} {B_CONTROL}

Interfaces

Sheet 20

Audio, video and external interfaces

{B_INTERFACES} {B_INTERFACES}

Mechanical

Sheet 28

Mechanical details and board documentation

{B_MECHANICAL} {B_MECHANICAL}

BUS ALIAS	SIGNALS / MEMBERS
B_ROOT	B_POWER, B_FPGA, B_CONTROL, B_INTERFACES, B_MECHANICAL

Precision-Arrays

Sheet: /
File: Minimig198itx.kicad_sch

Title: Minimig — System overview

Size: A4	Date: 2026-10-17	**Rev: 1.98itx**
KiCad E.D.A. 10.0.7		Id: 1/33

Power input, protection and rails

atx

Sheet 3

ATX power and front panel

{B_ATX} {B_ATX}

main power

Sheet 4

Power input and buck regulator

{B_MAIN_POWER} {B_MAIN_POWER}

regulated rails

Sheet 5

Regulated rails — 3.3 V, 1.25 V and 2.5 V

{B_REGULATED_RAILS} {B_REGULATED_RAILS}

{B_POWER}

BUS ALIAS	SIGNALS / MEMBERS
B_POWER	B_ATX, B_MAIN_POWER, B_REGULATED_RAILS

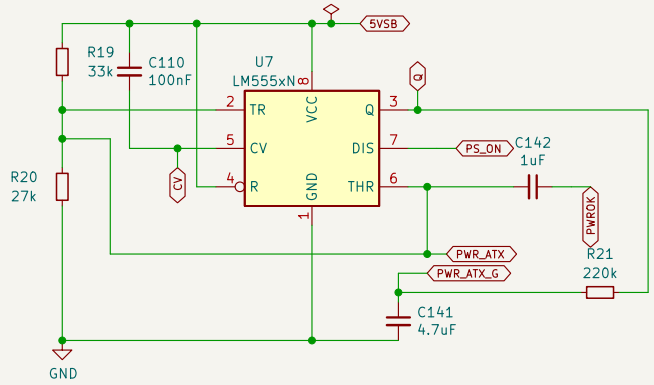
Precision-Arrays

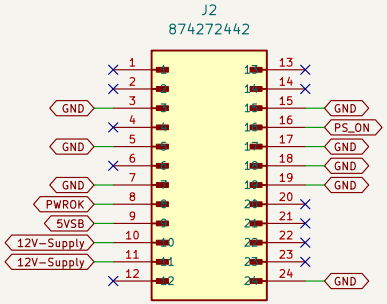
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File: Power.kicad_sch

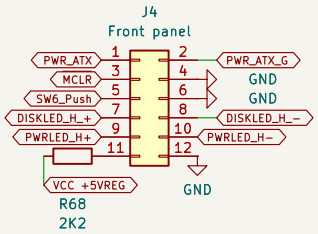
Title: Minimig — Power input, protection and rails

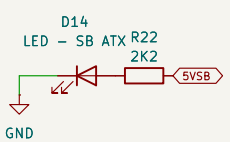
Size: A4	Date: 2026-10-17	**Rev: 1.98itx**
KiCad E.D.A. 10.0.7		Id: 2/33

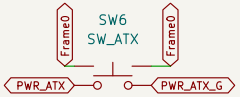
ATX power and front panel

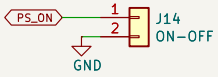












{B_ATX}

BUS ALIAS	SIGNALS / MEMBERS
B_ATX	12V-Supply, DISKLED_H_+, DISKLED_H_-, Frame0, GND, PWRLED_H+, PWRLED_H- SW6_Push, VCC +5VREG, MCLR

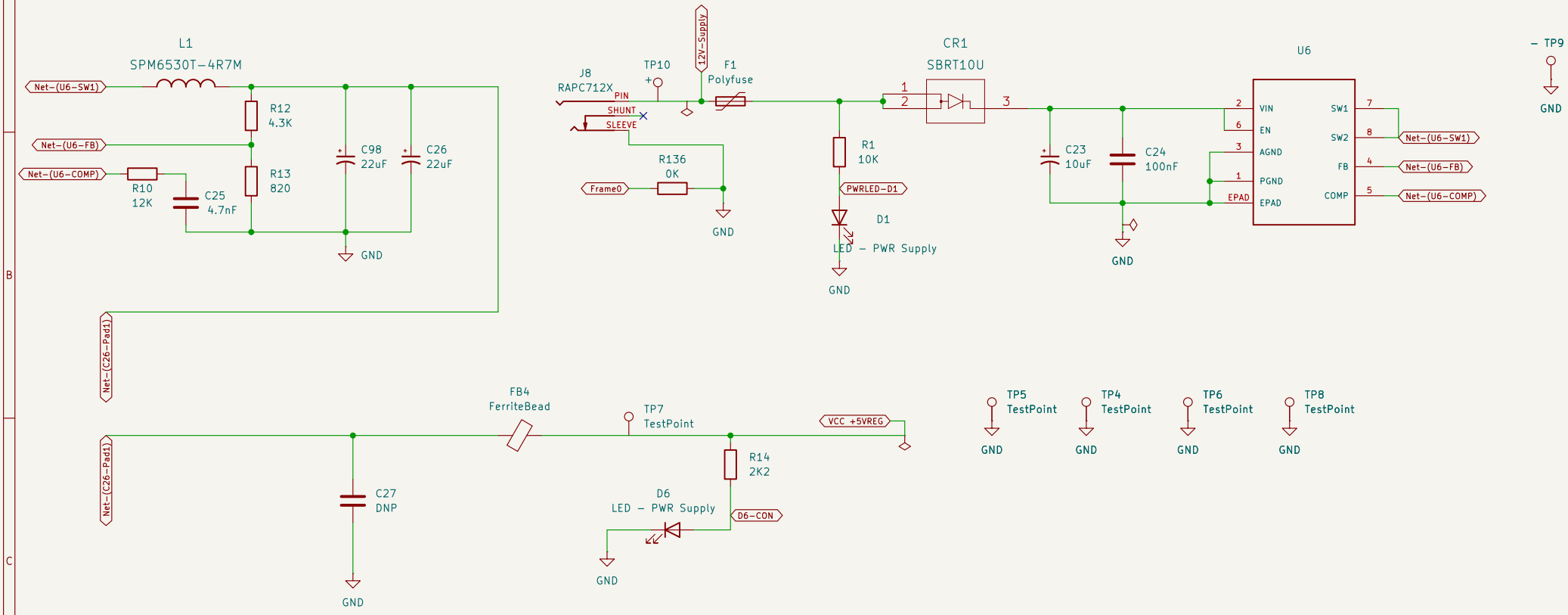
Precision-Arrays

Sheet: /Power/atx/
File: atx.kicad_sch

Title: Minimig - ATX power and front panel

Size: A4	Date: 2026-10-17	**Rev: 1.98itx**
KiCad E.D.A. 10.0.7		Id: 3/33

Power input and buck regulator



{B_MAIN_POWER}

BUS ALIAS	SIGNALS / MEMBERS
B_MAIN_POWER	12V-Supply, Frame0, GND, VCC +5VREG

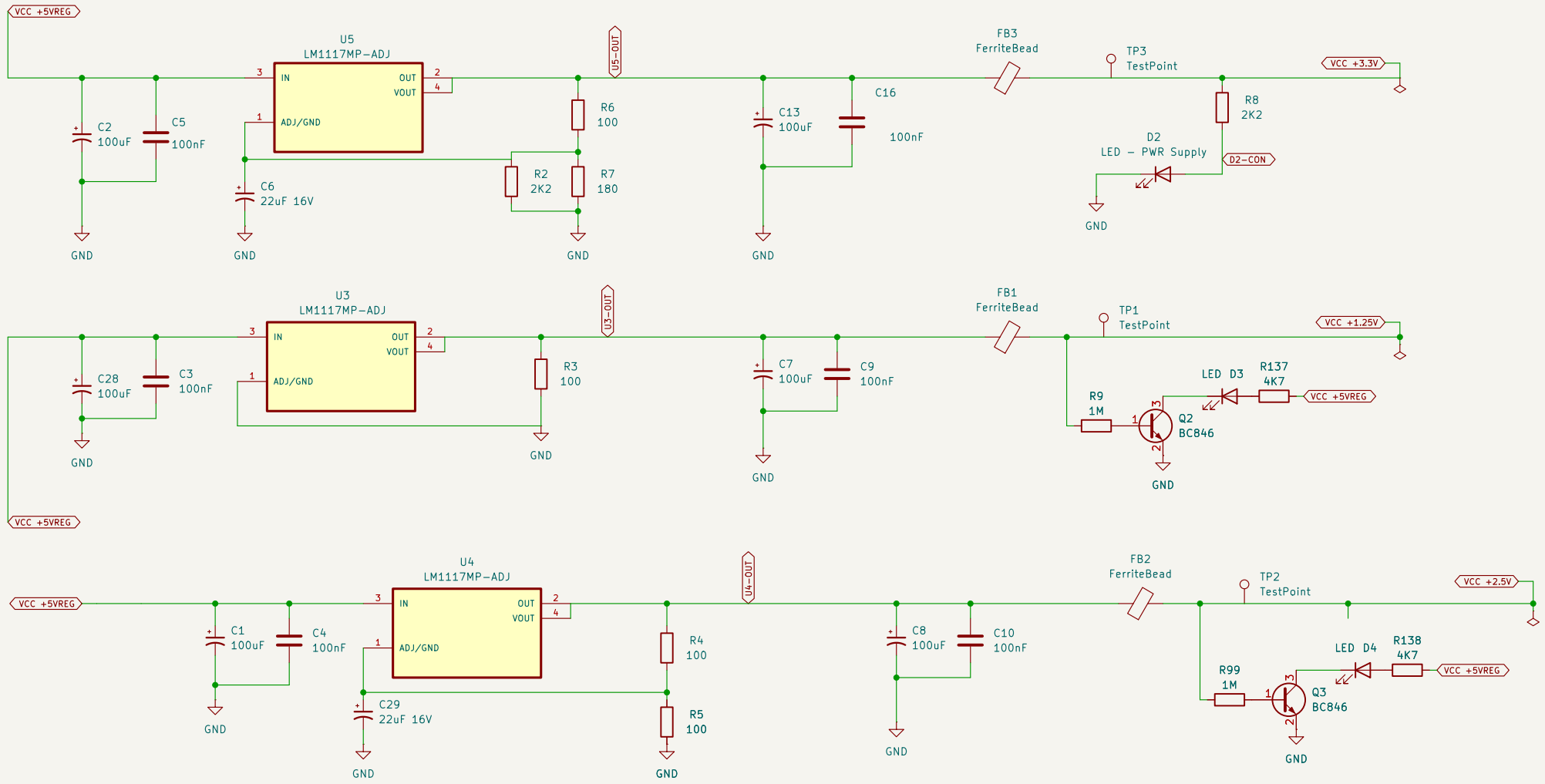
Precision-Arrays

Sheet: /Power/main power/
File: main_power.kicad_sch

Title: Minimig - Power input and buck regulator

Size: A4	Date: 2026-10-17	**Rev: 1.98itx**
KiCad E.D.A. 10.0.7		Id: 4/33

Regulated rails — 3.3 V, 1.25 V and 2.5 V



{B_REGULATED_RAILS}

BUS ALIAS	SIGNALS / MEMBERS
B_REGULATED_RAILS	GND, VCC +1.25V, VCC +2.5V, VCC +3.3V, VCC +5VREG

Precision-Arrays

Sheet: /Power/regulated rails/
File: regulated_rails.kicad_sch

Title: Minimig — Regulated rails — 3.3 V, 1.25 V and 2.5 V

Size: A4	Date: 2026-10-17	**Rev: 1.98itx**
KiCad E.D.A. 10.0.7		Id: 5/33

Spartan-3, clocks and memory

fpga cpu

Sheet 7

Spartan-3 — MC68000 interface

{B_FPGA_CPU} {B_FPGA_CPU}

fpga sram

Sheet 8

Spartan-3 — Asynchronous SRAM interface

{B_FPGA_SRAM} {B_FPGA_SRAM}

fpga video audio

Sheet 9

Spartan-3 — Video and audio outputs

{B_FPGA_VIDEO_AUDIO} {B_FPGA_VIDEO_AUDIO}

fpga user io

Sheet 10

Spartan-3 — Joysticks, PS/2 and serial

{B_FPGA_USER_IO} {B_FPGA_USER_IO}

fpga configuration

Sheet 11

Spartan-3 — Configuration, control and master clock

{B_FPGA_CONFIGURATION} {B_FPGA_CONFIGURATION}

fpga power

Sheet 12

Spartan-3 — Power, ground and supply bypass

{B_FPGA_POWER} {B_FPGA_POWER}

sram 1

Sheet 13

Asynchronous SRAM — 6 MiB (1/2)

{B_SRAM_1} {B_SRAM_1}

sram 2

Sheet 14

Asynchronous SRAM — 6 MiB (2/2)

{B_SRAM_2} {B_SRAM_2}

{B_FPGA}

BUS ALIAS	SIGNALS / MEMBERS
B_FPGA	B_FPGA_CPU, B_FPGA_SRAM, B_FPGA_VIDEO_AUDIO, B_FPGA_USER_IO B_FPGA_CONFIGURATION, B_FPGA_POWER, B_SRAM_1, B_SRAM_2

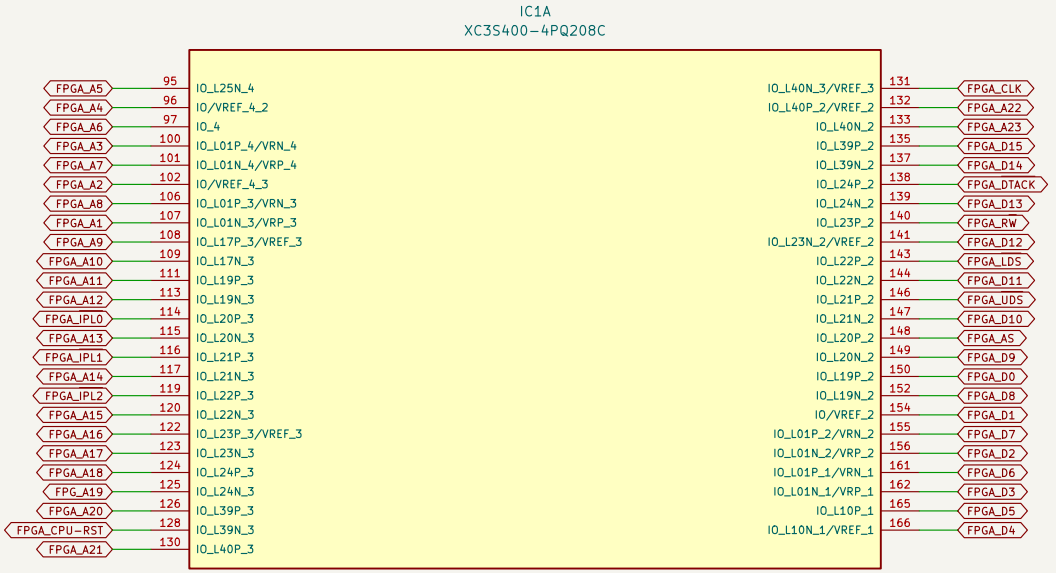
Precision-Arrays

Sheet: /FPGA/
File: FPGA.kicad_sch

Title: Minimig — Spartan-3, clocks and memory

Size: A4	Date: 2026-10-17	**Rev: 1.98itx**
KiCad E.D.A. 10.0.7		Id: 6/33

Spartan-3 — MC68000 interface



{B_FPGA_CPU}

BUS ALIAS	SIGNALS / MEMBERS
B_FPGA_CPU	FPGA_AS, FPGA_A[1..18], FPGA_A[20..23], FPGA_CLK, FPGA_CPU-RST, FPGA_D[0..15] FPGA_RW, FPGA_DTACK, FPGA_IPL0, FPGA_IPL1, FPGA_IPL2 FPGA_LDS, FPGA_UDS, FPG_A19

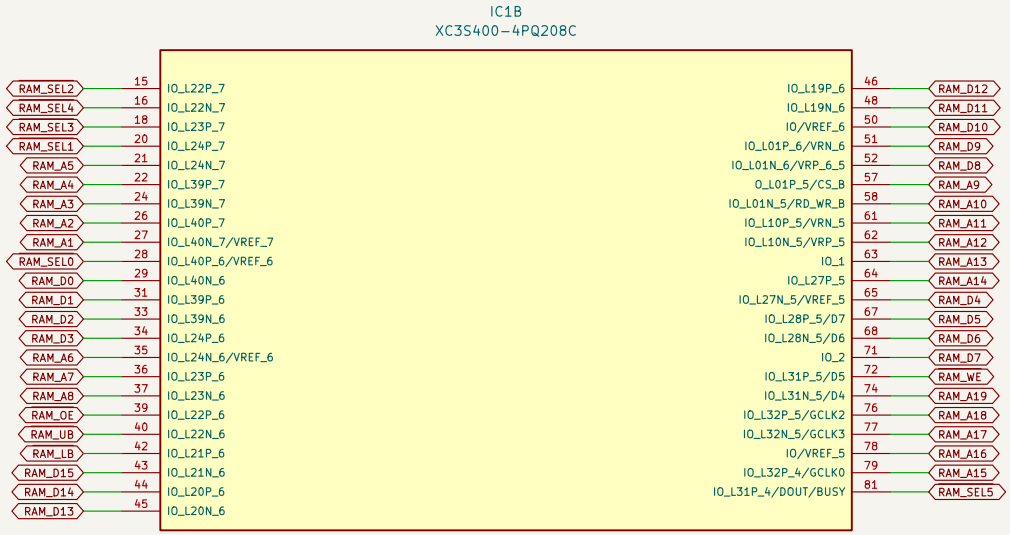
Precision-Arrays

Sheet: /FPGA/fpga cpu/
File: fpga_cpu.kicad_sch

Title: Minimig — Spartan-3 — MC68000 interface

Size: A4	Date: 2026-10-17	**Rev: 1.98itx**
KiCad E.D.A. 10.0.7		Id: 7/33

Spartan-3 — Asynchronous SRAM interface



{B_FPGA_SRAM}

BUS ALIAS	SIGNALS / MEMBERS
B_FPGA_SRAM	RAM_A[1..19], RAM_D[0..15], RAM_LB, RAM_OE, RAM_SEL0, RAM_SEL1 RAM_SEL2, RAM_SEL3, RAM_SEL4, RAM_SEL5, RAM_UB, RAM_WE

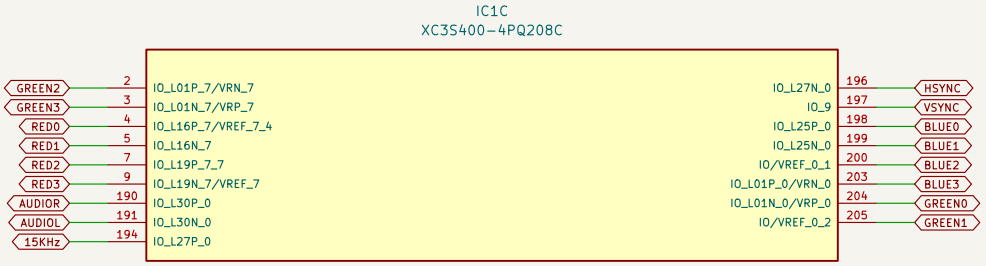
Precision-Arrays

Sheet: /FPGA/fpga sram/
File: fpga_sram.kicad_sch

Title: Minimig — Spartan-3 — Asynchronous SRAM interface

Size: A4	Date: 2026-10-17	**Rev: 1.98itx**
KiCad E.D.A. 10.0.7		Id: 8/33

Spartan-3 — Video and audio outputs



{B_FPGA_VIDEO_AUDIO}

BUS ALIAS	SIGNALS / MEMBERS
B_FPGA_VIDEO_AUDIO	15KHz, AUDIOL, AUDIOR, BLUE[0..3], GREEN[0..3], HSYNC, RED[0..3], VSYNC

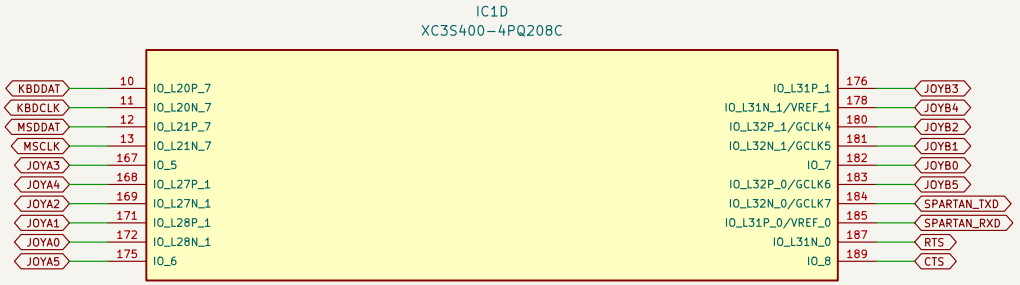
Precision-Arrays

Sheet: /FPGA/fpga video audio/
File: fpga_video_audio.kicad_sch

Title: Minimig — Spartan-3 — Video and audio outputs

Size: A4	Date: 2026-10-17	**Rev: 1.98itx**
KiCad E.D.A. 10.0.7		Id: 9/33

Spartan-3 – Joysticks, PS/2 and serial



{B_FPGA_USER_IO}

BUS ALIAS	SIGNALS / MEMBERS
B_FPGA_USER_IO	CTS, JOYA[0..5], JOYB[0..5], KBDCLK, KBDDAT, MSCLK, MSDDAT, RTS, SPARTAN_RXD SPARTAN_TXD

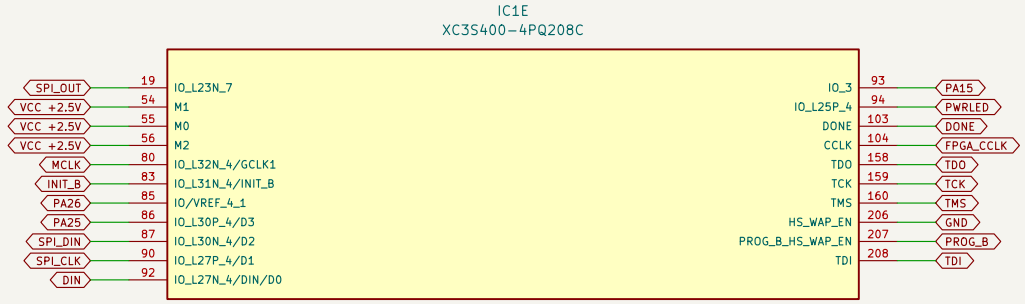
Precision-Arrays

Sheet: /FPGA/fpga user io/
File: fpga_user_io.kicad_sch

Title: Minimig – Spartan-3 – Joysticks, PS/2 and serial

Size: A4	Date: 2026-10-17	**Rev: 1.98itx**
KiCad E.D.A. 10.0.7		Id: 10/33

Spartan-3 — Configuration, control and master clock



{B_FPGA_CONFIGURATION}

BUS ALIAS	SIGNALS / MEMBERS
B_FPGA_CONFIGURATION	DIN, DONE, FPGA_CCLK, GND, INIT_B, MCLK, PA15, PA25, PA26, PROG_B, PWRLED SPI_CLK, SPI_DIN, SPI_OUT, TCK, TDI, TDO, TMS, VCC +2.5V

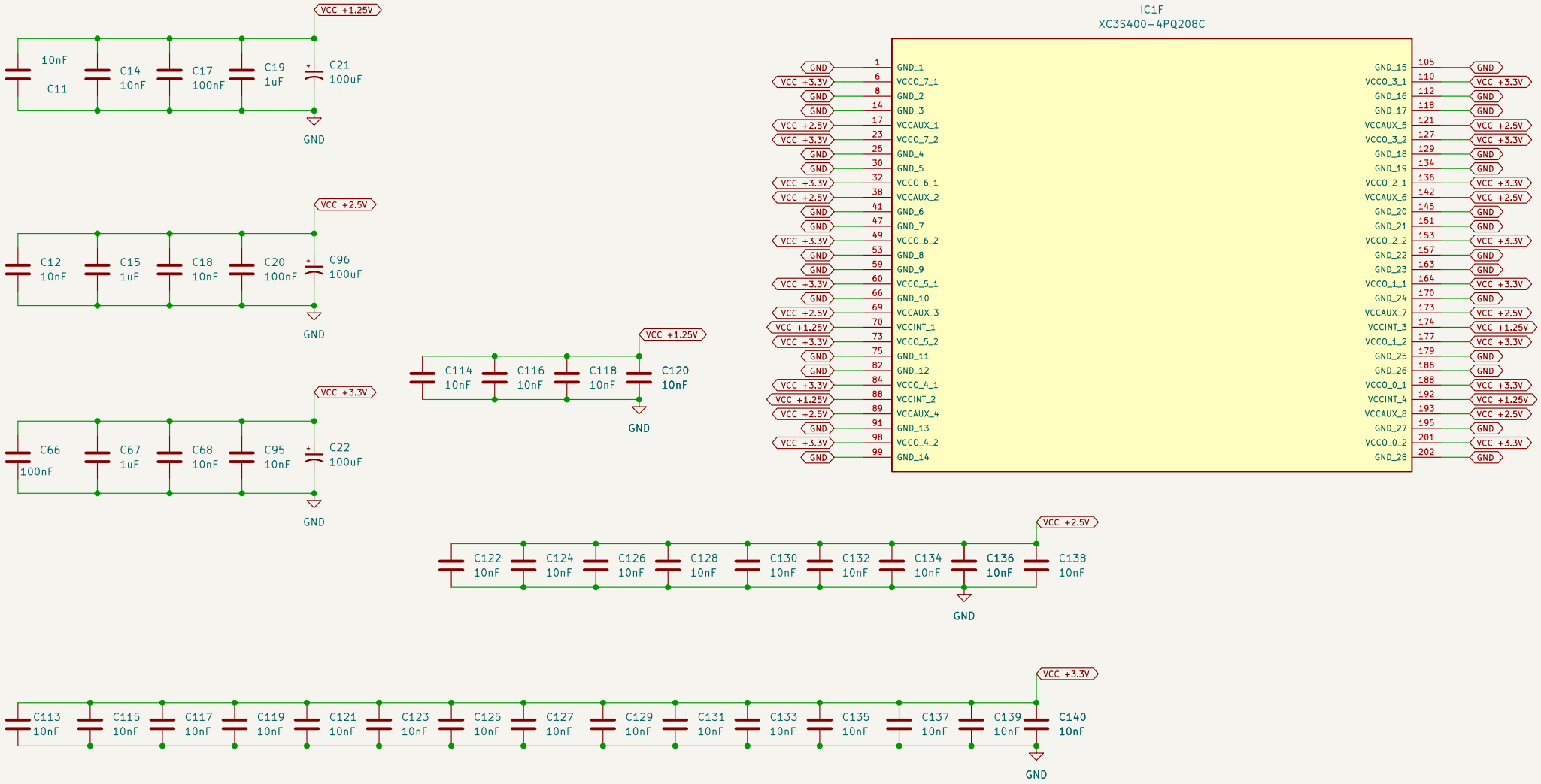
Precision-Arrays

Sheet: /FPGA/fpga configuration/
File: fpga_configuration.kicad_sch

Title: Minimig — Spartan-3 — Configuration, control and master clock

Size: A4	Date: 2026-10-17	**Rev: 1.98itx**
KiCad E.D.A. 10.0.7		Id: 11/33

Spartan-3 — Power, ground and supply bypass



{B_FPGA_POWER}

BUS ALIAS	SIGNALS / MEMBERS
B_FPGA_POWER	GND, VCC +1.25V, VCC +2.5V, VCC +3.3V

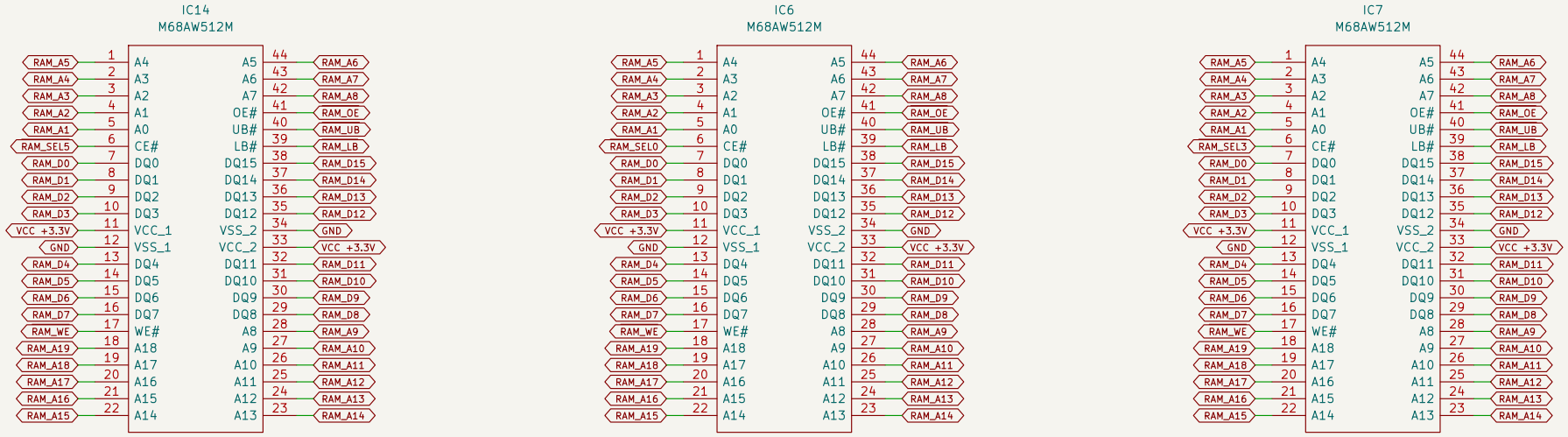
Precision-Arrays

Sheet: /FPGA/fpga power/
File: fpga_power.kicad_sch

Title: Minimig — Spartan-3 — Power, ground and supply bypass

Size: A4	Date: 2026-10-17	**Rev: 1.98itx**
KiCad E.D.A. 10.0.7		Id: 12/33

Asynchronous SRAM — 6 MiB (1/2)



{B_SRAM_1}

BUS ALIAS	SIGNALS / MEMBERS
B_SRAM_1	GND, RAM_A[1..19], RAM_D[0..15], VCC, +3.3V, RAM_LB, RAM_OE, RAM_SEL0 RAM_SEL3, RAM_SEL5, RAM_UB, RAM_WE

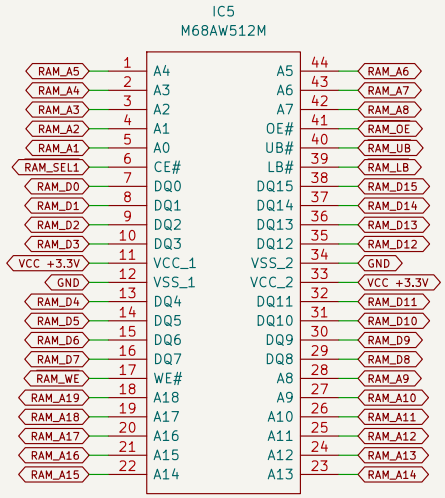
Precision-Arrays

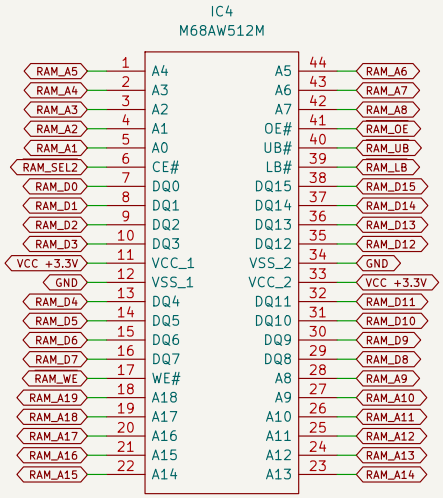
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File: sram_1.kicad_sch

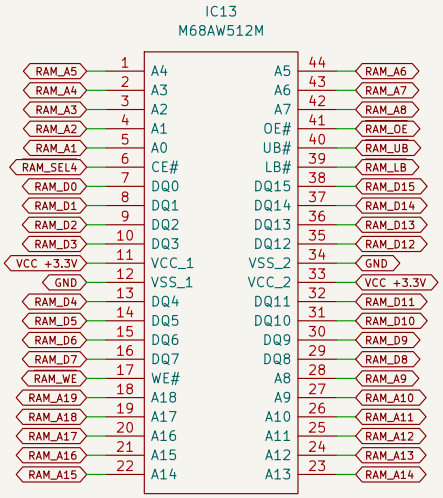
Title: Minimig — Asynchronous SRAM — 6 MiB (1/2)

Size: A4	Date: 2026-10-17	**Rev: 1.98itx**
KiCad E.D.A. 10.0.7		Id: 13/33

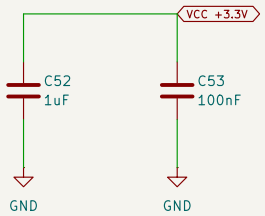
Asynchronous SRAM — 6 MiB (2/2)



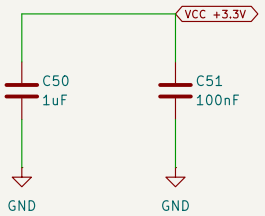




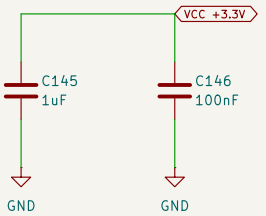
IC5 supply bypass



IC4 supply bypass



IC13 supply bypass



{B_SRAM_2}

BUS ALIAS	SIGNALS / MEMBERS
B_SRAM_2	GND, RAM_A[1..19], RAM_D[0..15], VCC, +3.3V, RAM_LB, RAM_OE, RAM_SEL1 RAM_SEL2, RAM_SEL4, RAM_UB, RAM_WE

Precision-Arrays

Sheet: /FPGA/sram 2/
File: sram_2.kicad_sch

Title: Minimig — Asynchronous SRAM — 6 MiB (2/2)

Size: A4	Date: 2026-10-17	**Rev: 1.98itx**
KiCad E.D.A. 10.0.7		Id: 14/33

MC68000, ARM and storage

cpu core

Sheet 16

MC68000, supply bypass and bus pull-ups

{B_CPU_CORE} {B_CPU_CORE}

cpu translators

Sheet 17

MC68000 bus translation — IC8 to IC12

{B_CPU_TRANSLATORS} {B_CPU_TRANSLATORS}

mcu core

Sheet 18

AT91SAM7S256, clock and local controls

{B_MCU_CORE} {B_MCU_CORE}

mcu usb sd

Sheet 19

ARM USB, boot and microSD

{B_MCU_USB_SD} {B_MCU_USB_SD}

{B_CONTROL}

BUS ALIAS	SIGNALS / MEMBERS
B_CONTROL	B_CPU_CORE, B_CPU_TRANSLATORS, B_MCU_CORE, B_MCU_USB_SD

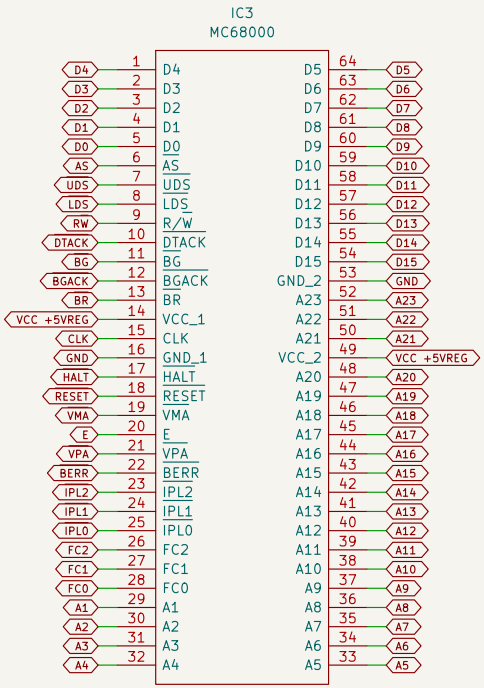
Precision-Arrays

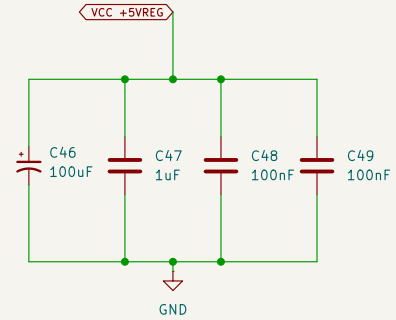
Sheet: /Control/
File: Control.kicad_sch

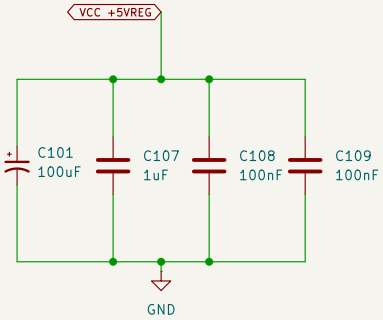
Title: Minimig — MC68000, ARM and storage

Size: A4	Date: 2026-10-17	**Rev: 1.98itx**
KiCad E.D.A. 10.0.7		Id: 15/33

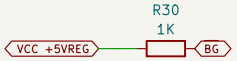
MC68000, supply bypass and bus pull-ups



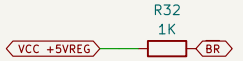


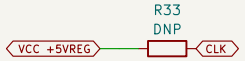


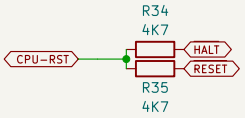


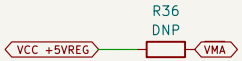




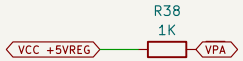






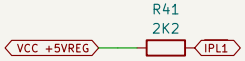




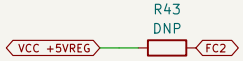


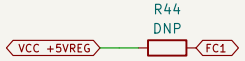






















{B_CPU_CORE}

BUS ALIAS	SIGNALS / MEMBERS
B_CPU_CORE	AS, A[1..23], CLK, CPU-RST, D[0..15], GND, R/W, VCC +5VREG, DTACK IPL0, IPL1, IPL2, LDS, UDS

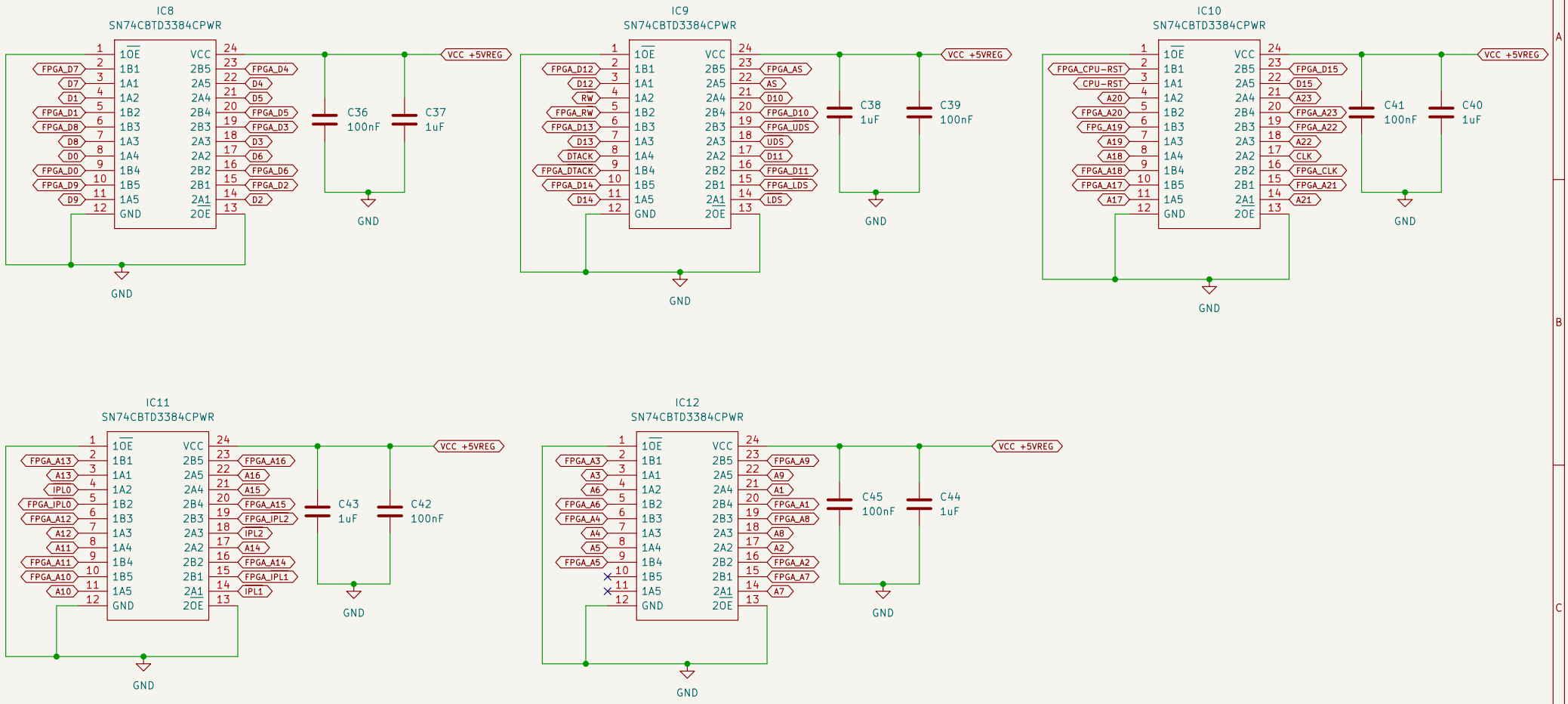
Precision-Arrays

Sheet: /Control/cpu core/
File: cpu_core.kicad_sch

Title: Minimig — MC68000, supply bypass and bus pull-ups

Size: A4	Date: 2026-10-17	**Rev: 1.98itx**
KiCad E.D.A. 10.0.7		Id: 16/33

MC68000 bus translation — IC8 to IC12



{B_CPU_TRANSLATORS}

BUS ALIAS	SIGNALS / MEMBERS
B_CPU_TRANSLATORS	AS, A[1..23], CLK, CPU-RST, D[0..15], FPGA_AS, FPGA_A[1..18], FPGA_A[20..23] FPGA_CLK, FPGA_CPU-RST, FPGA_D[0..15], FPGA_RW, FPGA_DTACK FPGA_IPL0, FPGA_IPL1, FPGA_IPL2, FPGA_LDS, FPGA_UDS, FPG_A19 GND, RW, VCC +5VREG, DTACK, IPL0, IPL1, IPL2, LDS, UDS

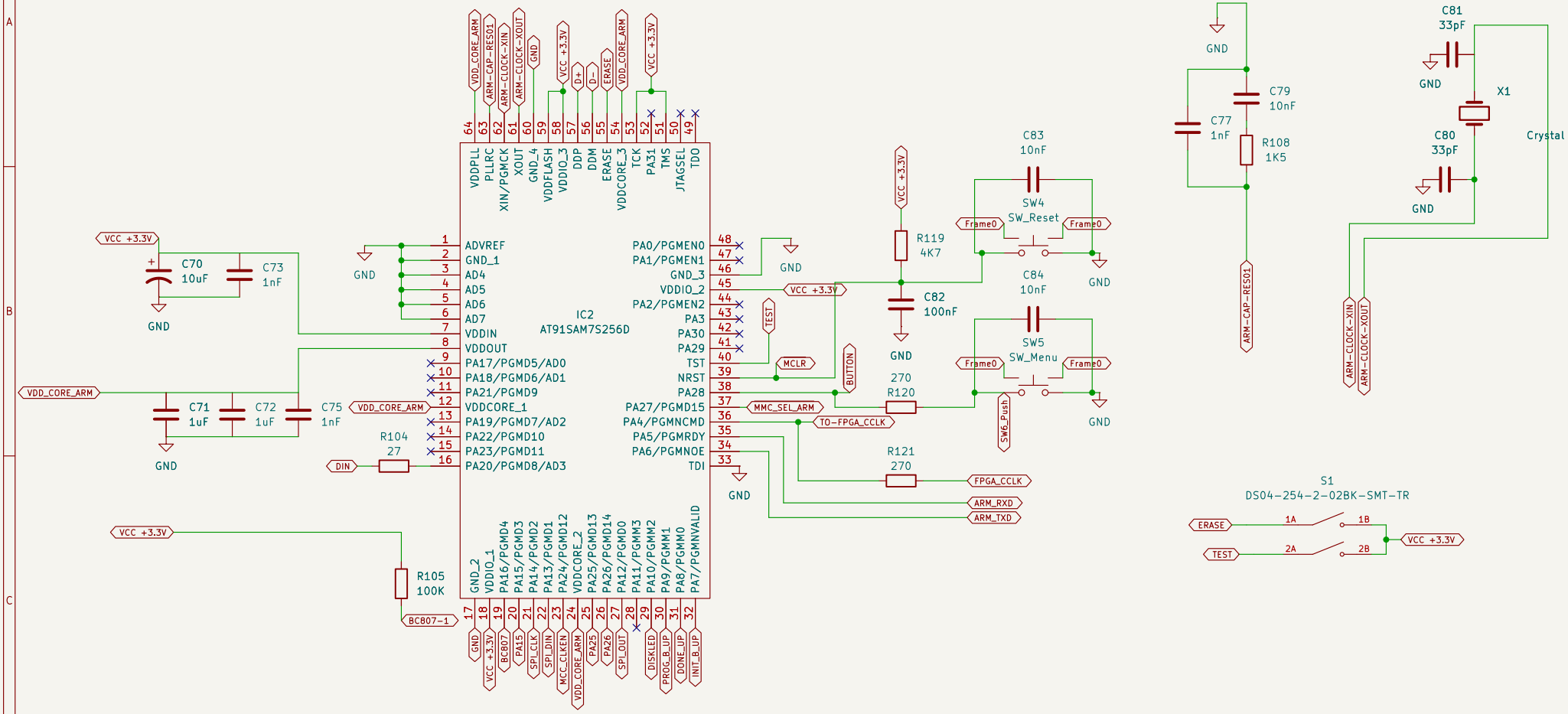
Precision-Arrays

Sheet: /Control/cpu translators/
File: cpu_translators.kicad_sch

Title: Minimig — MC68000 bus translation — IC8 to IC12

Size: A4	Date: 2026-10-17	**Rev: 1.98itx**
KiCad E.D.A. 10.0.7		Id: 17/33

AT91SAM7S256, clock and local controls



{B_MCU_CORE}

BUS ALIAS	SIGNALS / MEMBERS
B_MCU_CORE	ARM_RXD, ARM_TXD, BC807, BC807-1, D+, D-, DIN, DISKLED, DONE_UP, FPGA_CCLK Frame0, GND, INIT_B_UP, MCC_CLKEN, PA15, PA25, PA26, PROG_B_UP, SPI_CLK SPI_DIN, SPI_OUT, SW6_Push, VCC +3.3V, VDD_CORE_ARM, MCLR, MMC_SEL_ARM

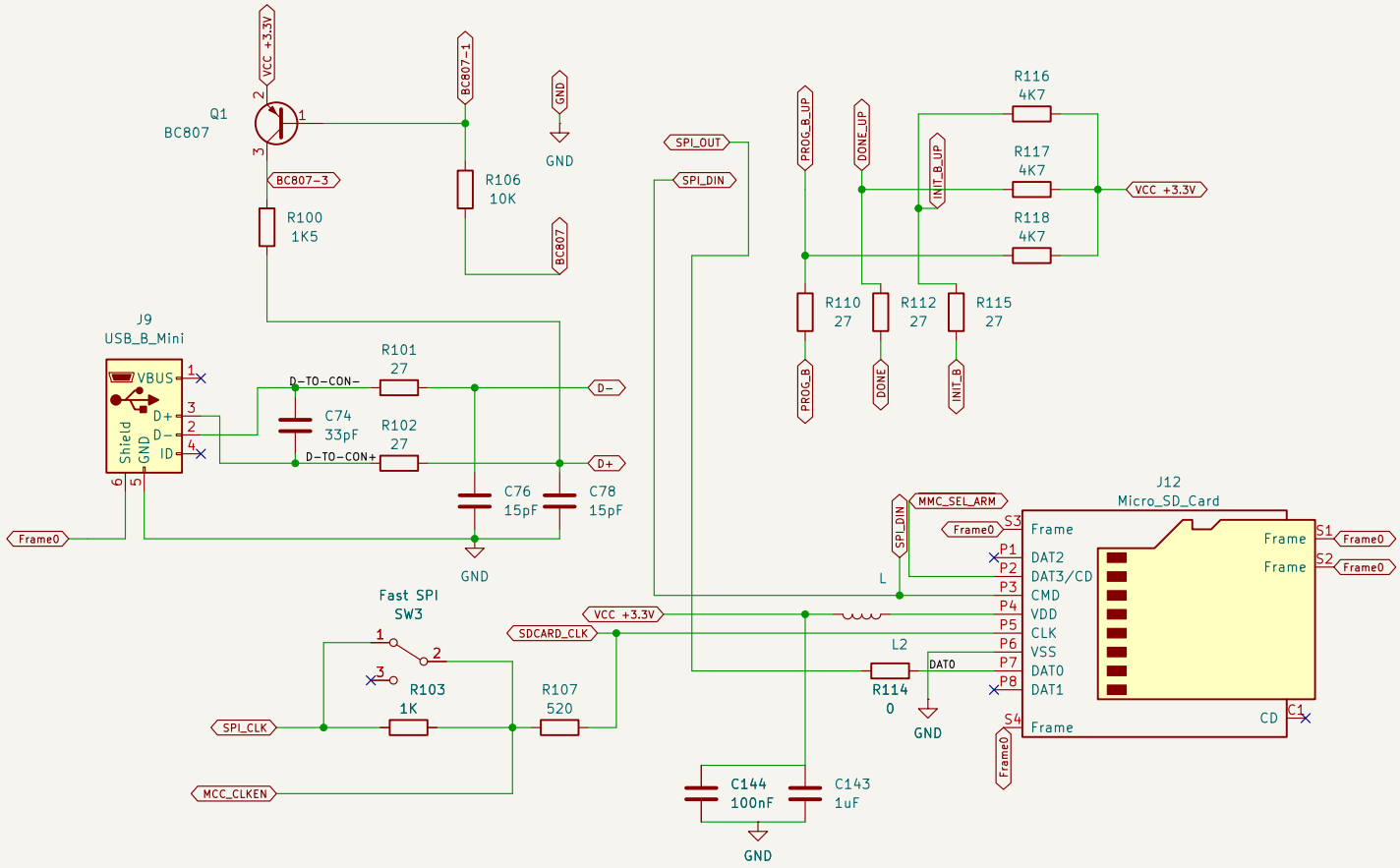
Precision-Arrays

Sheet: /Control/mcu core/
File: mcu_core.kicad_sch

Title: Minimig — AT91SAM7S256, clock and local controls

Size: A4	Date: 2026-10-17	**Rev: 1.98itx**
KiCad E.D.A. 10.0.7		Id: 18/33

ARM USB, boot and microSD



{B_MCU_USB_SD}

BUS ALIAS	SIGNALS / MEMBERS
B_MCU_USB_SD	BC807, BC807-1, D+, D-, DONE, DONE_UP, Frame0, GND, INIT_B, INIT_B_UP MCC_CLKEN, PROG_B, PROG_B_UP, SPI_CLK, SPI_DIN, SPI_OUT, VCC +3.3V MMC_SEL_ARM

Precision-Arrays

Sheet: /Control/mcu usb sd/
File: mcu_usb_sd.kicad_sch

Title: Minimig — ARM USB, boot and microSD

Size: A4	Date: 2026-10-17	**Rev: 1.98itx**
KiCad E.D.A. 10.0.7		Id: 19/33

Audio, video and external interfaces

audio

Sheet 21

Stereo audio output

{B_AUDIO} {B_AUDIO}

clock

Sheet 22

clock

{B_CLOCK} {B_CLOCK}

controller

Sheet 23

controller

{B_CONTROLLER} {B_CONTROLLER}

joystick

Sheet 24

joystick

{B_JOYSTICK} {B_JOYSTICK}

ps2

Sheet 25

PS/2 keyboard and mouse

{B_PS2} {B_PS2}

serial

Sheet 26

RS-232 and ESP-01 interfaces

{B_SERIAL} {B_SERIAL}

vga

Sheet 27

VGA DAC, sync and supply bypass

{B_VGA} {B_VGA}

{B_INTERFACES}

BUS ALIAS	SIGNALS / MEMBERS
B_INTERFACES	B_AUDIO, B_CLOCK, B_CONTROLLER, B_JOYSTICK, B_PS2, B_SERIAL, B_VGA

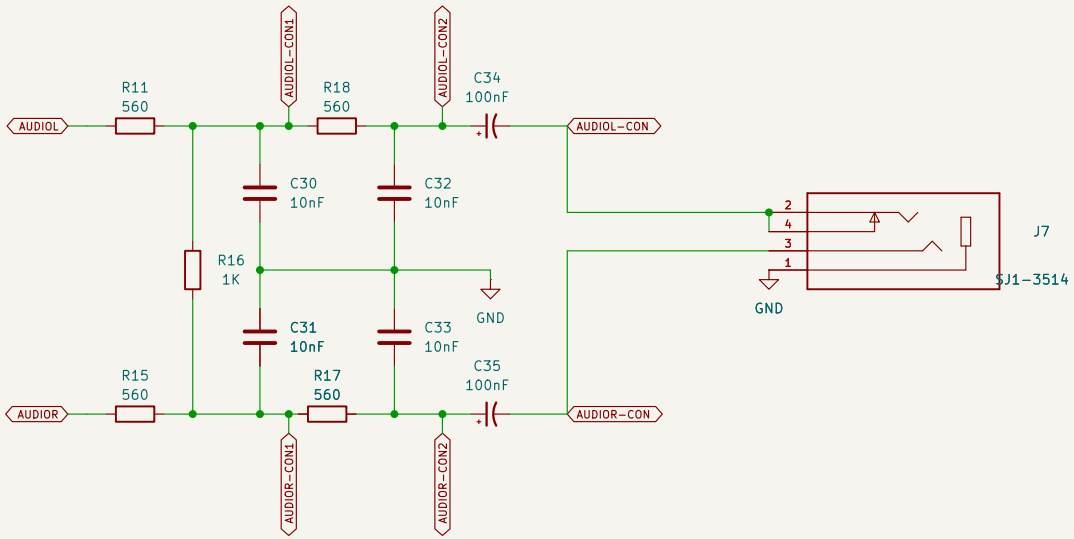
Precision-Arrays

Sheet: /Interfaces/
File: Interfaces.kicad_sch

Title: Minimig — Audio, video and external interfaces

Size: A4	Date: 2026-10-17	**Rev: 1.98itx**
KiCad E.D.A. 10.0.7		Id: 20/33

Stereo audio output



{B_AUDIO}

BUS ALIAS	SIGNALS / MEMBERS
B_AUDIO	AUDIOL, AUDIOR, GND

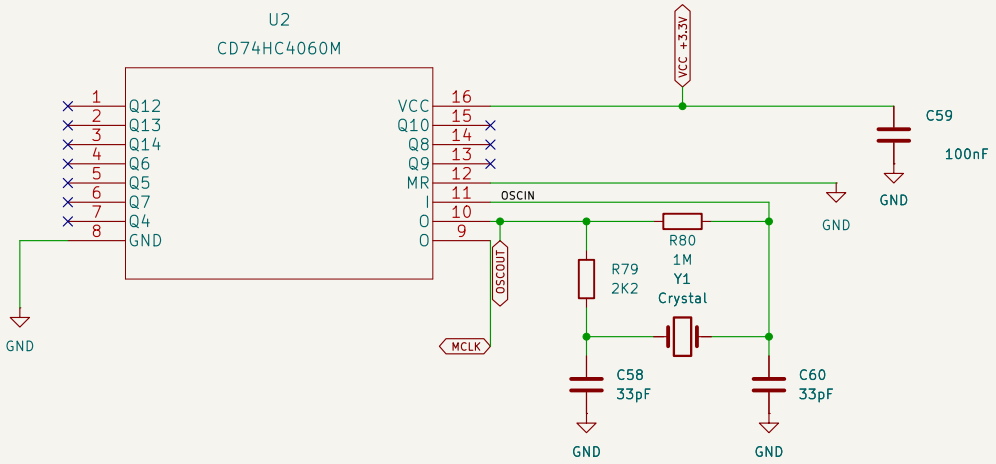
Precision-Arrays

Sheet: /Interfaces/audio/
File: audio.kicad_sch

Title: Minimig — Stereo audio output

Size: A4	Date: 2026-10-17	**Rev: 1.98itx**
KiCad E.D.A. 10.0.7		Id: 21/33

clock



{B_CLOCK}

BUS ALIAS	SIGNALS / MEMBERS
B_CLOCK	GND, MCLK, VCC +3.3V

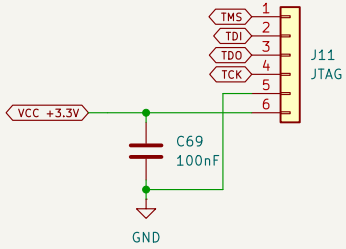
Precision-Arrays

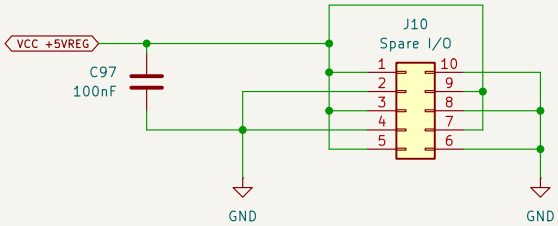
Sheet: /Interfaces/clock/
File: clock.kicad_sch

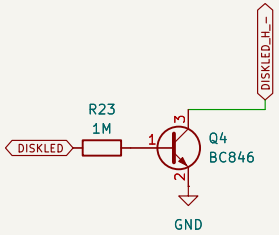
Title: Minimig — clock

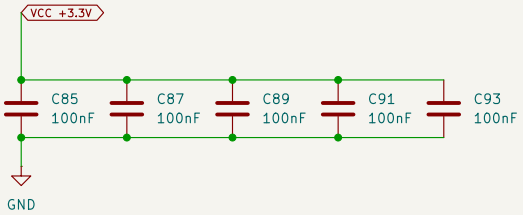
Size: A4	Date: 2026-10-17	**Rev: 1.98itx**
KiCad E.D.A. 10.0.7		Id: 22/33

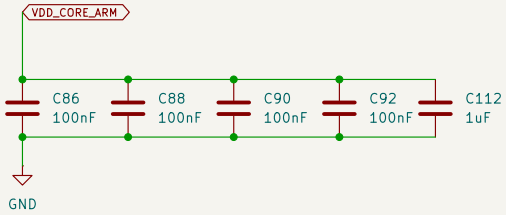
controller

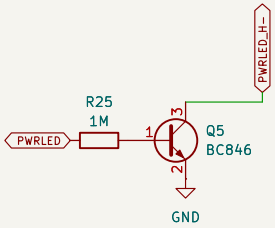


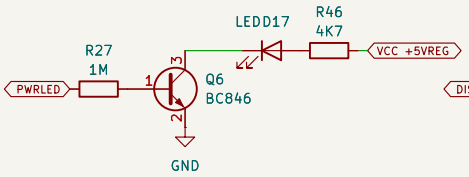


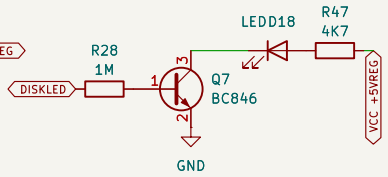


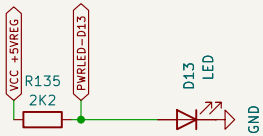


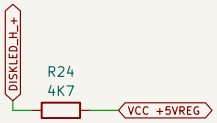


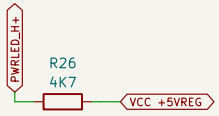












{B_CONTROLLER}

BUS ALIAS	SIGNALS / MEMBERS
B_CONTROLLER	DISKLED, DISKLED_H_+, DISKLED_H_-, GND, PWRLED, PWRLED_H+, PWRLED_H-, TCK TDI, TDO, TMS, VCC +3.3V, VCC +5VREG, VDD_CORE_ARM

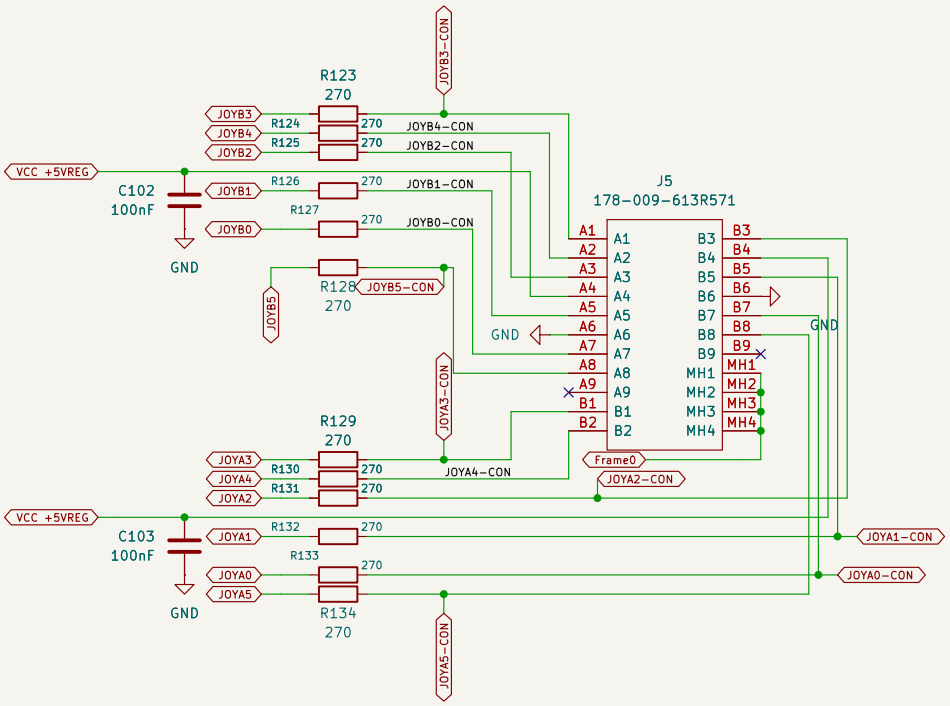
Precision-Arrays

Sheet: /Interfaces/controller/
File: controller.kicad_sch

Title: Minimig — controller

Size: A4	Date: 2026-10-17	**Rev: 1.98itx**
KiCad E.D.A. 10.0.7		Id: 23/33

joystick



{B_JOYSTICK}

BUS ALIAS	SIGNALS / MEMBERS
B_JOYSTICK	Frame0, GND, JOYA[0..5], JOYB[0..5], VCC +5VREG

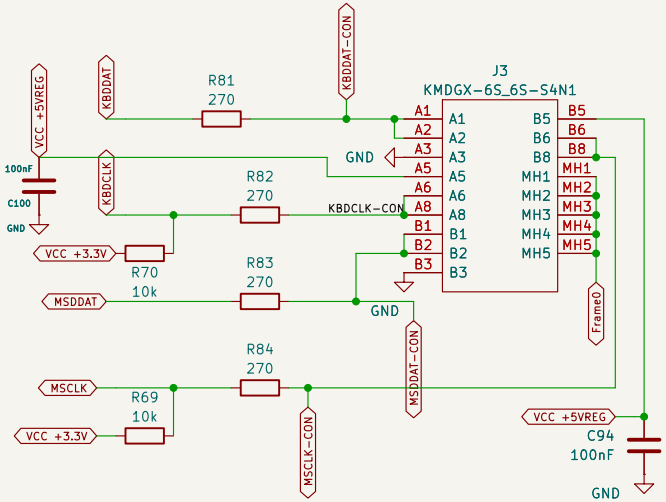
Precision-Arrays

Sheet: /Interfaces/joystick/
File: joystick.kicad_sch

Title: Minimig — joystick

Size: A4	Date: 2026-10-17	**Rev: 1.98itx**
KiCad E.D.A. 10.0.7		Id: 24/33

PS/2 keyboard and mouse



{B_PS2}

BUS ALIAS	SIGNALS / MEMBERS
B_PS2	Frame0, GND, KBDCLK, KBDDAT, MSCLK, MSDDAT, VCC +3.3V, VCC +5VREG

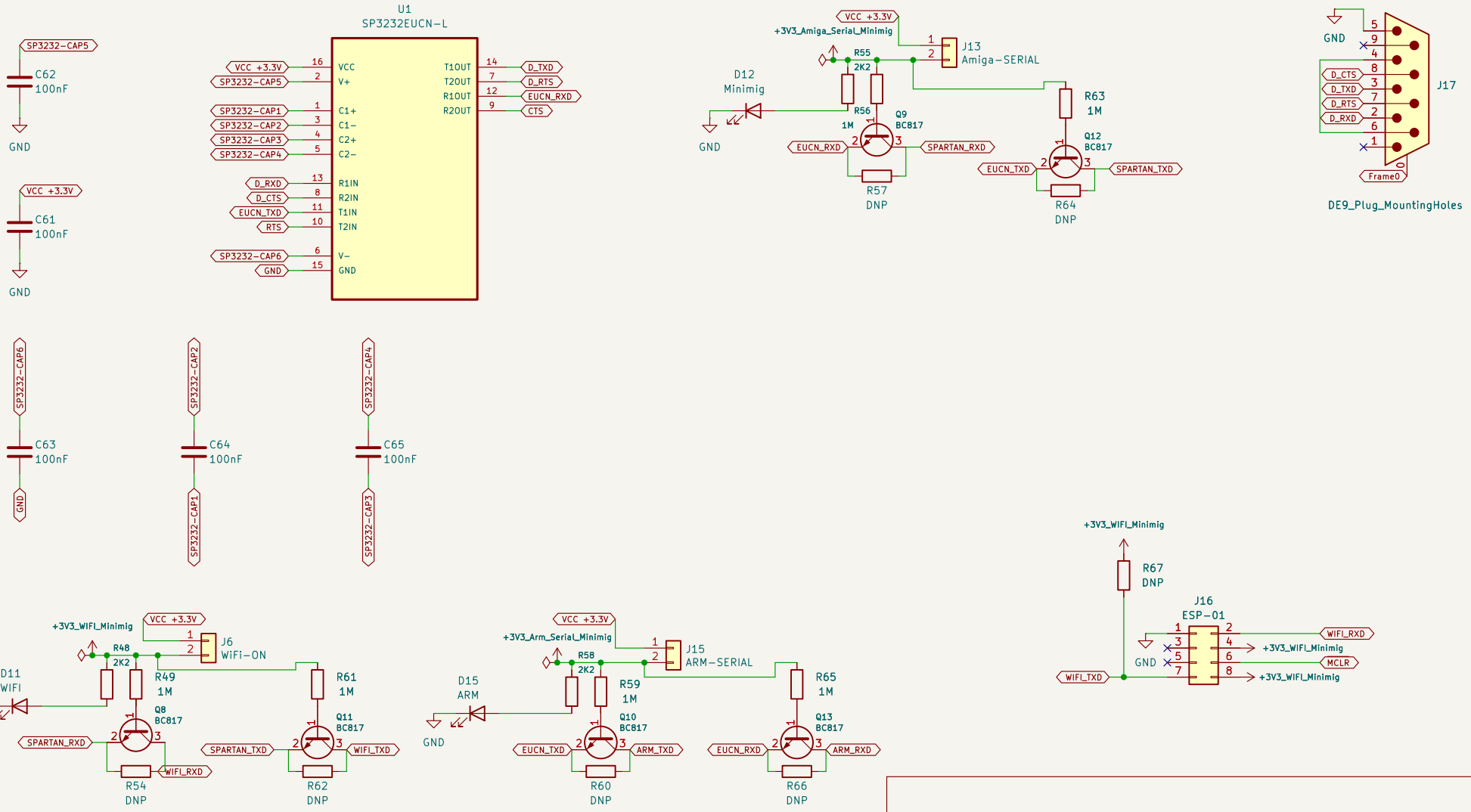
Precision-Arrays

Sheet: /Interfaces/ps2/
File: ps2.kicad_sch

Title: Minimig — PS/2 keyboard and mouse

Size: A4	Date: 2026-10-17	**Rev: 1.98itx**
KiCad E.D.A. 10.0.7		Id: 25/33

RS-232 and ESP-01 interfaces



{B_SERIAL}

BUS ALIAS	SIGNALS / MEMBERS
B_SERIAL	ARM_RXD, ARM_TXD, CTS, Frame0, GND, RTS, SPARTAN_RXD, SPARTAN_TXD, VCC +3.3V MCLR

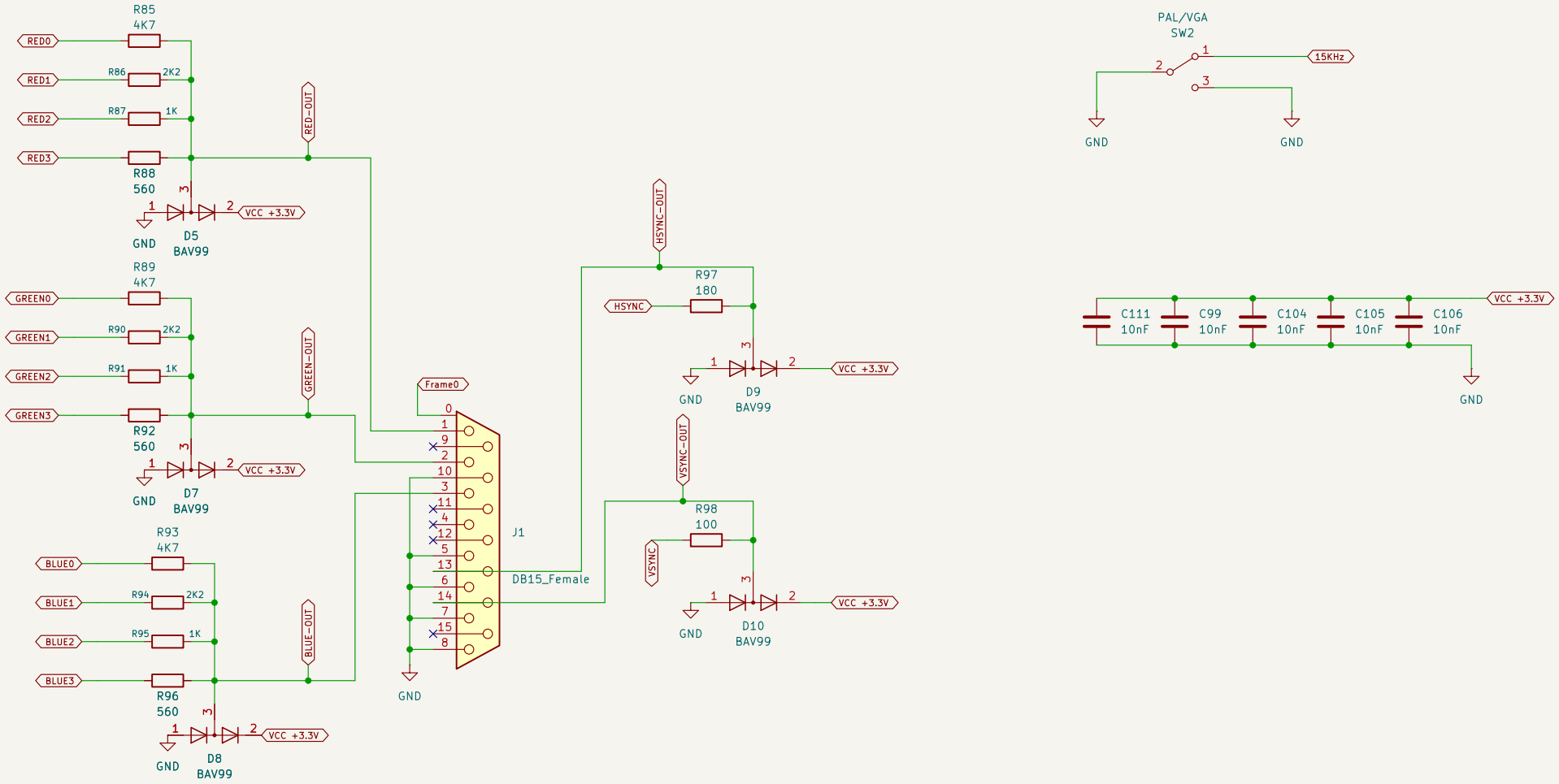
Precision-Arrays

Sheet: /Interfaces/serial/
File: serial.kicad_sch

Title: Minimig — RS-232 and ESP-01 interfaces

Size: A4	Date: 2026-10-17	**Rev: 1.98itx**
KiCad E.D.A. 10.0.7		Id: 26/33

VGA DAC, sync and supply bypass



{B_VGA}

BUS ALIAS	SIGNALS / MEMBERS
B_VGA	15KHz, BLUE[0..3], Frame0, GND, GREEN[0..3], HSYNC, RED[0..3], VCC +3.3V VSYNC

Precision-Arrays

Sheet: /Interfaces/vga/
File: vga.kicad_sch

Title: Minimig — VGA DAC, sync and supply bypass

Size: A4	Date: 2026-10-17	**Rev: 1.98itx**
KiCad E.D.A. 10.0.7		Id: 27/33

Mechanical details and board documentation

Top assembly

Sheet 29

Top assembly

Bottom assembly

Sheet 30

Bottom assembly

Stackup & fabrication

Sheet 31

Stackup & fabrication

Routing & impedance

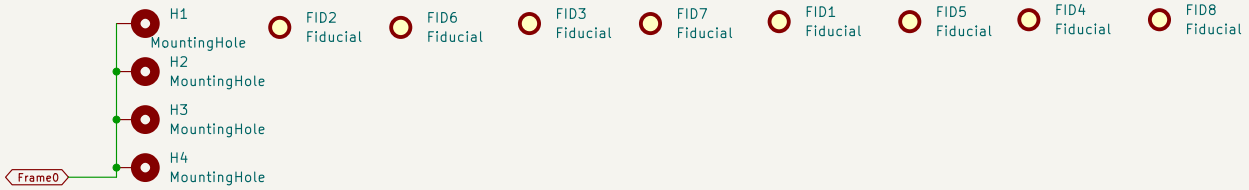
Sheet 32

Routing & impedance

Power & signal identification

Sheet 33

Power & signal identification



{B_MECHANICAL}

BUS ALIAS	SIGNALS / MEMBERS
B_MECHANICAL	Frame0

Precision-Arrays

Sheet: /Mechanical/
File: Mechanical.kicad_sch

Title: Minimig — Mechanical details and board documentation

Size: A4	Date: 2026-10-17	**Rev: 1.98itx**
KiCad E.D.A. 10.0.7		Id: 28/33

Top assembly

Placement plan, fitted-side orientation and native 3D reference

ASSEMBLY NOTES

01 View from outside the top. Orient using the board outline and connector edges.

02 Reference plan: 1:2 at A4 / 100%. The 170 mm board is drawn 85 mm wide.

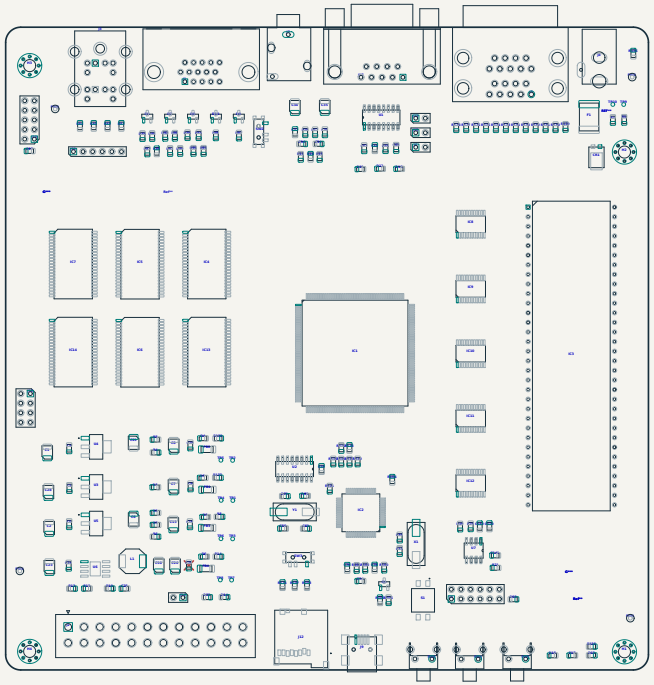
03 Teal marks pad 1 / A1. Check polarity and pin numbering against the footprint.

04 Red crosses mark saved DNP values. There are 18 options; native DNP flags are unset.

05 IC1: Spartan-3. IC2: ARM controller. IC3: MC68000. IC8-12: bus translation.

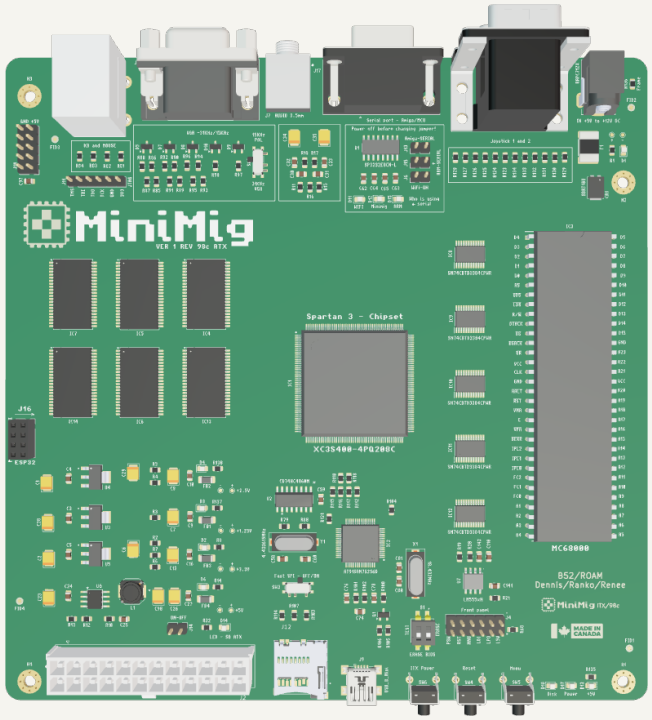
06 IC4-7 / IC13-14: six SRAMs, 6 MiB total. Shared 16-bit data and 19 address signals.

REFERENCE PLAN / 1:2



25 mm print check

3D ASSEMBLY VIEW



Side	Qty	SMD	DNP
Top	217	172	1
Bottom	175	175	17

Ref	Role	Device
IC1	FPGA / PQ208	XC3S400-4PQ208C
IC2	Controller	AT91SAM7S256D
IC3	CPU / DIP64	MC68000

Dennis, Ranko, Renee / Minimig.ca / Precision-Arrays

Revision 1.98itx | 2026-10-17 | PCB 2d3f20eb0dd8

Units: mm. Saved CAD governs. 3D views are illustrative.

A4 landscape. Print at 100% for the stated drawing scales.

Documentation only; no electrical symbols

Minimig.ca / Minimig

Sheet: /Mechanical/Top assembly/

File: AssemblyTop.kicad_sch

Title: Minimig — Top assembly

Size: A4	Date: 2026-10-17	**Rev: 1.98itx**
KiCad E.D.A. 10.0.7		Id: 29/33

Bottom assembly

Placement plan, fitted-side orientation and native 3D reference

ASSEMBLY NOTES

01 View from outside the bottom. Bottom view is mirrored left to right.

02 Reference plan: 1:2 at A4 / 100%. The 170 mm board is drawn 85 mm wide.

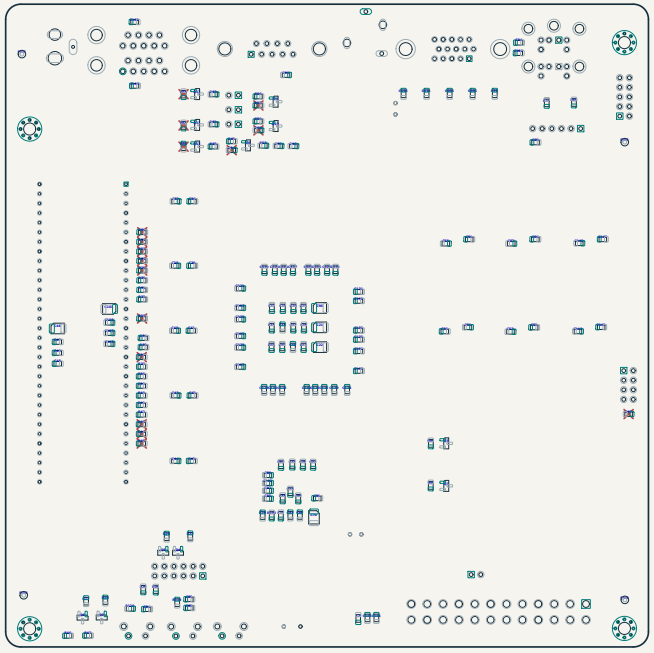
03 Teal marks pad 1 / A1. Check polarity and pin numbering against the footprint.

04 Red crosses mark saved DNP values. There are 18 options; native DNP flags are unset.

05 IC1: Spartan-3. IC2: ARM controller. IC3: MC68000. IC8-12: bus translation.

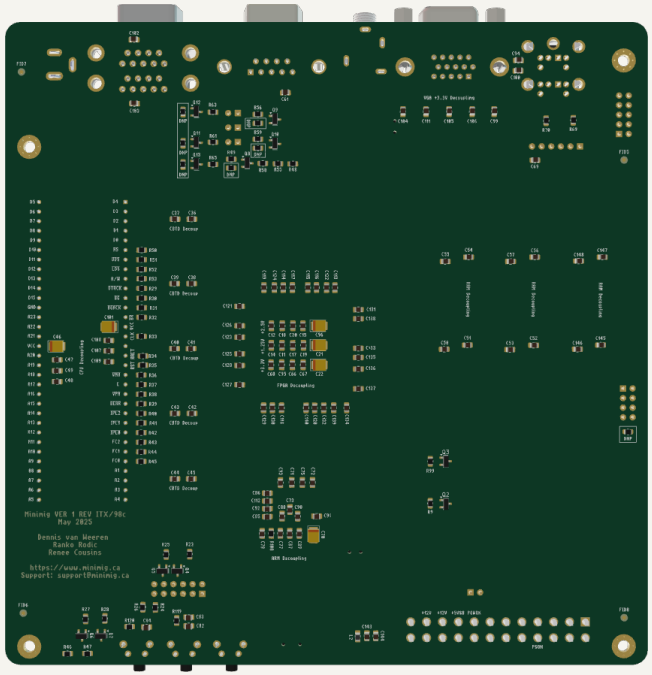
06 IC4-7 / IC13-14: six SRAMs, 6 MiB total. Shared 16-bit data and 19 address signals.

REFERENCE PLAN / 1:2



25 mm print check

3D ASSEMBLY VIEW



Ref	Drill	X	Y
H1	3.2	163.65	165.20
H2	3.2	163.65	33.02
H3	3.2	6.35	10.16
H4	3.2	6.35	165.10

Mounting holes H1-4 connect to Frame0. Outline: 170 × 170 mm, R4 corners; nominal thickness 1.6 mm. FID1-4 are on top; FID5-8 are on the bottom.

Hole coordinates use the top-view upper-left outline tangent: +X right, +Y down. This table is not mirrored.

Dennis, Ranko, Renee / Minimig.ca / Precision-Arrays

Revision 1.98itx | 2026-10-17 | PCB 2d3f20eb0dd8

Units: mm. Saved CAD governs. 3D views are illustrative.

A4 landscape. Print at 100% for the stated drawing scales.

Documentation only; no electrical symbols

Minimig.ca / Minimig

Sheet: /Mechanical/Bottom assembly/

File: AssemblyBottom.kicad_sch

Title: Minimig — Bottom assembly

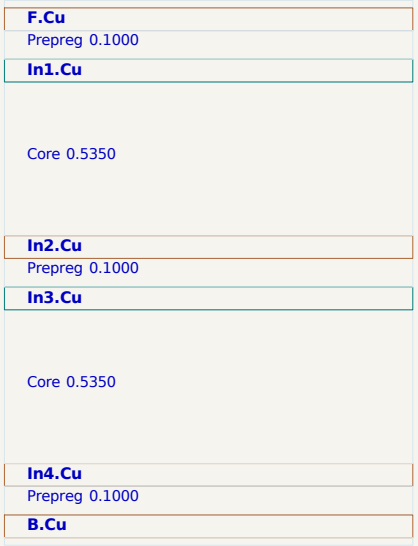
Size: A4	Date: 2026-10-17	**Rev: 1.98itx**
KiCad E.D.A. 10.0.7		Id: 30/33

Stackup & fabrication

Saved laminate definition, copper allocation and through-via inventory

6 COPPER LAYERS

Thickness exaggerated



Layer	Material	t (mm)	Er	Df	Saved role
F.Mask	Mask	0.01	—	—	Coating
F.Cu	Copper	0.035	—	—	Signals / power
dielectric 1	FR4	0.1	4.5	0.02	Insulation
In1.Cu	Copper	0.035	—	—	GND reference
dielectric 2	FR4	0.535	4.5	0.02	Insulation
In2.Cu	Copper	0.035	—	—	Signals / power
dielectric 3	FR4	0.1	4.5	0.02	Insulation
In3.Cu	Copper	0.035	—	—	GND reference
dielectric 4	FR4	0.535	4.5	0.02	Insulation
In4.Cu	Copper	0.035	—	—	Signals / power
dielectric 5	FR4	0.1	4.5	0.02	Insulation
B.Cu	Copper	0.035	—	—	GND label; signal routing
B.Mask	Mask	0.01	—	—	Coating

Thickness sum: 1.600 mm with masks; 1.580 mm without masks.

FR4: Er 4.5 / Df 0.02. All copper layers: 0.035 mm.

Saved finish: None. No specific laminate or impedance target.

THROUGH VIAS

Land Ø	Drill Ø	Annulus	Count
0.45	0.2	0.125	767

In1 and In3 are ground references. B.Cu is named GND but also carries signals; inspect copper and return paths. Confirm stack, finish and drill capability before fabrication.

767 routing vias. Component and mounting drills are separate.

Dennis, Ranko, Renee / Minimig.ca / Precision-Arrays

Revision 1.98itx | 2026-10-17 | PCB 2d3f20eb0dd8

Units: mm. Saved CAD governs. 3D views are illustrative.

A4 landscape. Print at 100% for the stated drawing scales.

Documentation only; no electrical symbols

Minimig.ca / Minimig

Sheet: /Mechanical/Stackup & fabrication/
File: Stackup.kicad_sch

Title: Minimig — Stackup & fabrication

Size: A4	Date: 2026-10-17	**Rev: 1.98itx**
KiCad E.D.A. 10.0.7		Id: 31/33

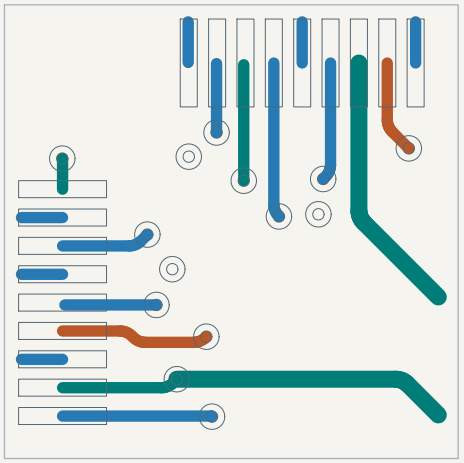
Routing & impedance

Saved widths and native copper details; dimensions in millimetres

Circuit / rule	Width	Gap	Saved evidence
MC68000 bus	0.200	—	49 used channels through IC8-12
Asynchronous SRAM	0.200	—	Six devices; shared address and 16-bit data bus
VGA RGB / sync	0.200	—	Four resistor-DAC bits per colour
USB service D+ / D−	0.200	—	Mini-B J9 to ARM IC2; VBUS unconnected
Default netclass	0.250	0.250	Clearance 0.150; diff-pair width 0.200
Power / minimum	0.200–3.000	—	Power widths vary; minimum rule 0.200

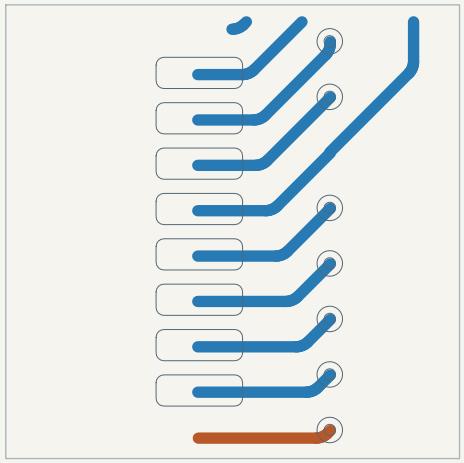
No per-interface impedance target is saved. Colours identify nets; they do not impose routing constraints.

A / FPGA LEAD ESCAPE



F.Cu / 7.5:1

B / SRAM BUS DETAIL



F.Cu / 7.5:1; native curves

REFERENCE PLANES

In1 and In3: ground reference. F.Cu, In2 and In4: signals and power. B.Cu also has signal routing.

SRAM: RAM_D0–15, RAM_A1–19 and separate RAM_SEL0–5 selects. There is no SDRAM clock interface.

Preserve return paths and decoupling. These details record geometry; they do not establish skew, matched lengths or impedance.

Blue: signals

Orange: power; teal: ground

Dennis, Ranko, Renee / Minimig.ca / Precision-Arrays

Revision 1.98itx | 2026-10-17 | PCB 2d3f20eb0dd8

Units: mm. Saved CAD governs. 3D views are illustrative.

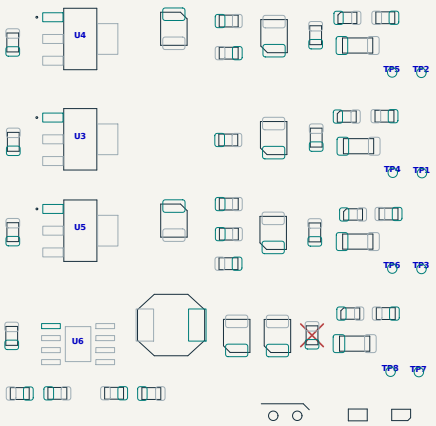
A4 landscape. Print at 100% for the stated drawing scales.

Documentation only; no electrical symbols
Minimig.ca / Minimig
Sheet: /Mechanical/Routing & impedance/
File: Routing.kicad_sch
Title: Minimig — Routing & impedance
Size: A4 | Date: 2026-10-17 | Rev: 1.98itx
KiCad E.D.A. 10.0.7 | Id: 32/33

Power & signal identification

Regulated-rail probe points, indicators and drawing colours

REGULATOR / PROBE LOCATOR



Top view / 1.25:1

RAILS & INPUT

Nominal rail	Regulator	LED	Probe + / GND
+1.25V	U3	D3	TP1 / TP4
+2.5V	U4	D4	TP2 / TP5
+3.3V	U5	D2	TP3 / TP6
+5VREG	U6	D6	TP7 / TP8
12V-Supply	Input	D1	TP10 / TP9

All probe pairs are on top. TP10 (+12 V) / TP9 (GND) are beside the barrel input. Rail names are nominal values, not acceptance tolerances.

D14: ATX standby. U7 / 5VSB: ATX control. Mini-USB VBUS is unconnected. J10 supplies +5VREG / GND despite its saved Spare I/O value.

BUS COLOUR KEY

- Power rails
- Ground / return
- MC68000 interface
- Shared SRAM bus
- FPGA / ARM control
- Video / sync
- Stereo audio
- Joystick / PS/2 / serial

Drawing colours are reading aids. The saved project has one Default netclass with transparent colour fields. Named nets and pin connectivity govern.

Input: 12 V via J2 ATX or J8 barrel. Simultaneous-source operation is not specified.

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Documentation only; no electrical symbols
Minimig.ca / Minimig
Sheet: /Mechanical/Power & signal identification/
File: PowerAndBuses.kicad_sch
Title: Minimig — Power & signal identification
Size: A4 | Date: 2026-10-17 | Rev: 1.98itx
KiCad E.D.A. 10.0.7 | Id: 33/33